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PTO/SB/05 (12/97)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 03692.P040D Total Pages 2

First Named Inventor or Application Identifier Balu Balakrishnan

Express Mail Label No. EL431687917US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 92)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 13)

4. X Oath or Declaration (Total Pages 5)
   a. ___ Newly Executed (Original or Copy)
   b. X Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__X__ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. __X__ a. Information Disclosure Statement (IDS)/PTO-1449
__X__ b. Copies of IDS Citations
12. __X__ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __X__ Other: separate sheet with title, express mail label, copy of postcard and attorney's signature

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation __X__ Divisional ____ Continuation-in-part (CIP)
of prior application No: 09/405,209

18. **Correspondence Address**
_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)
or
__X__ Correspondence Address Below

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FEE TRANSMITTAL FOR FY 2001

TOTAL AMOUNT OF PAYMENT ($) 710.00

Complete if Known:
Application No. New Application
Filing Date Herewith
First Named Inventor Balu Balakrishnan
Group Art Unit Not Yet Assigned
Examiner Name Not Yet Assigned
Attorney Docket No. 003692.P040D

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

   Deposit Account Number 02-2666
   Deposit Account Name

   [X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

2. X **Payment Enclosed:**
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   ____ **Money Order**
   ____ **Other**

FEE CALCULATION

1. **BASIC FILING FEE**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility application filing fee	710.00
106	320	206	160	Design application filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 710.00

2. **EXTRA CLAIM FEES**

		Extra Claims		Fee from below		Fee Paid
Total Claims***	12	– 20** =	0	X 18.00	=	0.00
Independent Claims***	2	– 3** =	0	X 80.00	=	0.00
Multiple Dependent					=	

**Or number previously paid, if greater; For Reissues, see below.
*** Number of claims remaining after preliminary amendment.

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 0.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	390	216	195	Extension for response within second month	
117	890	217	445	Extension for response within third month	
118	1,390	218	695	Extension for response within fourth month	
128	1,890	228	945	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,240	241	620	Petition to revive unintentionally abandoned application	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	710	249	355	For each additional invention to be examined (see 37 CFR 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify)					
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) $ 0.00

SUBMITTED BY:

Typed or Printed Name: James Y. Go

Signature: _____ Date: 10-26-00

Reg. Number: 40,621 Telephone Number: (425) 827-8600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Balu Balakrishnan et al.	)	Examiner: Not Yet Assigned
	)	
Serial No. New Application	)	Art Unit: Not Yet Assigned
	)	
Filed: Herewith	)	
	)	
For: METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTROLLER	)	

PRELIMINARY AMENDMENT

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination of the above referenced application, the Applicants respectfully request the Examiner to enter the following amendments and to consider the following remarks.

IN THE SPECIFICATION

On page 1, line 3, please insert the following:

--This is a Divisional of U.S. Application Serial No. 09/405,209, filed September 24, 1999, now pending.--

IN THE CLAIMS

Please cancel claims 1-11, 19-58, and 64-112 without prejudice:

REMARKS

The present application is a divisional of U.S. Application Serial No. 09/405,209. Claims 1-11, 19-58, and 64-112 are canceled herein. Claims 12-18 and 59-63 are now pending for examination. An IDS and fees to cover the pending claims are being submitted with this preliminary amendment. Allowance of all pending claims is earnestly solicited.

Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee due in this matter.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR and ZAFMAN

Dated: 10-26-00

James Y. Go
Reg. No. 40,621

"Express Mail" mailing label number: EL431687917US
Date of Deposit: October 26, 2000
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Rimma N. Oks
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Oks Rimma
(Signature of person mailing paper or fee) 10-26-00 (Date signed)

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTROLLER

Inventors: Balu Balakrishnan
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Attorney's Docket No.: 003692.P040

"Express Mail" mailing label number: EL431684867US
Date of Deposit September 24, 1999
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231
Melanie Besecker
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9-24-99
(Date signed)

METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTROLLER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to power supplies and, more specifically, the present invention relates to a switched mode power supply controller.

Background Information

Electronic devices use power to operate. Switched mode power supplies are commonly used due to their high efficiency and good output regulation to power many of today's electronic devices. In a known switched mode power supply, a low frequency (e.g. 50 Hz or 60 Hz mains frequency), high voltage alternating current (AC) is converted to high voltage direct current (DC) with a diode rectifier and capacitor. The high voltage DC is then converted to high frequency (e.g. 30 to 300 kHz) AC, using a switched mode power supply control circuit. This high frequency, high voltage AC is applied to a transformer to transform the voltage, usually to a lower voltage, and to provide safety isolation. The output of the transformer is rectified to provide a regulated DC output, which may be used to power an electronic device. The switched mode power supply control circuit provides usually output regulation by sensing the output controlling it in a closed loop.

A switched mode power supply may include an integrated circuit power supply controller coupled in series with a primary winding of the transformer. Energy is transferred to a secondary winding from the primary winding in a manner controlled by the power supply controller to provide the clean and steady source of power at the DC output. The transformer of a switched mode power supply may also include another winding called a bias or feedback winding. The bias winding provides the operating power for the power supply controller and in some cases it also provides a feedback or control signal to the power supply controller. In some switched mode power supplies, the feedback or control signal can come through an opto-coupler from a sense circuit coupled to the DC output. The feedback or control signal may be used to modulate a duty cycle of a switching waveform generated by the power supply controller or may be used to disable some of the cycles of the switching waveform generated by the power supply controller to control the DC output voltage.

A power supply designer may desire to configure the power supply controller of a switched mode power supply in a variety of different ways, depending on for example the particular application and/or operating conditions. For instance, there may be one application in which the power supply designer would like the power supply controller to have one particular functionality and there may be another application in which the power supply designer would like the power supply controller to have

another particular functionality. It would be convenient for power supply designer to be able to use the same integrated power supply controller for these different functions.

In order to provide the specific functions to the power supply controller, additional pins or electrical terminals are added for each function to the integrated circuit power supply controllers. Consequently, each additional function generally translates into an additional pin on the power supply controller chip, which translates into increased costs and additional external components. Another consequence of providing additional functionality to power supply controllers is that there is sometimes a substantial increase in power consumption by providing the additional functionality.

SUMMARY OF THE INVENTION

Power supply controller methods and apparatuses are disclosed. In one embodiment, a power supply controller circuit is described including a current input circuit coupled to receive a current. In one embodiment, the current input circuit is to generate an enable/disable signal in response to the current. The power supply controller is to activate and deactivate the power supply in response to the enable/disable signal. In another embodiment, a current limit of a power switch of the power supply controller is adjusted in response to the current. In yet another embodiment, a maximum duty cycle of the power switch of the power supply is adjusted in response to the current. Additional features and benefits of the present invention will become apparent from the detailed description, figures and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention detailed illustrated by way of example and not limitation in the accompanying figures.

Figure 1 is a schematic illustrating one embodiment of a power supply including a power supply controller having a multi-function terminal in accordance with the teachings of the present invention.

Figure 2A is a schematic illustrating one embodiment of a power supply controller having a multi-function terminal configured to limit the current of the power switch in the power supply controller to a desired value in accordance with the teachings of the present invention.

Figure 2B is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide a switchable on/off control to the power supply in accordance with the teachings of the present invention.

Figure 2C is a schematic illustrating one embodiment of the power supply having a multi-function terminal configured to limit the current of the power switch in the power supply controller to a desired value and provide a switchable on/off control to the power supply controller in accordance with the teachings of the present invention.

Figure 2D is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide line under-voltage detection, line over-voltage detection and maximum duty cycle

reduction of the power supply in accordance with the teachings of the present invention.

Figure 2E is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide line under-voltage detection, line over-voltage detection, maximum duty cycle reduction and a switchable on/off control to the power supply in accordance with the teachings of the present invention.

Figure 2F is a schematic illustrating one embodiment of current mode control of a power supply controller having a multi-function terminal configured to regulate the current limit of the power switch in response to the power supply output in accordance with the teachings of the present invention.

Figure 3 is a block diagram illustrating one embodiment of a power supply controller including a multi-function terminal in accordance with teachings of the present invention.

Figure 4 is a schematic illustrating one embodiment of a power supply controller including a multi-function terminal in accordance with the teachings of the present invention.

Figure 5 is a diagram illustrating one embodiment of currents, voltages and duty cycles in relation to current through a multi-function terminal of a power supply controller in accordance with teachings of the present invention.

Figure 6A is a diagram illustrating one embodiment of timing diagrams of switching waveforms of a power supply controller including a multi-function terminal in accordance with teachings of the present invention.

Figure 6B is a diagram illustrating another embodiment of timing diagrams of switching waveforms of the power supply controller including a multi-function terminal in accordance with teachings of the present invention.

Figure 7 is a schematic illustrating another embodiment of a power supply controller including a multi-function terminal in accordance with the teachings of the present invention.

Figure 8 is a diagram illustrating another embodiment of timing diagrams of switching waveforms of the power supply controller including a multi-function terminal in accordance with teachings of the present invention.

DETAILED DESCRIPTION

A method and an apparatus providing a multi-function terminal in a power supply controller is disclosed. In the following description, numerous specifically details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

In one embodiment of the present invention, a power supply controller is provided with the functionality of being able to remotely turn on and off the power supply. In another embodiment, the power supply controller is provided with the functionality of being able to externally set the current limit of a power switch in the power supply controller, which makes it easier to prevent saturation of the transformer reducing transformer size and cost. Externally settable current limit also allows the maximum power output to be kept constant over a wide input range reducing the cost of components that would otherwise have to handle the excessive power at high input voltages. In yet another embodiment, the power supply controller is provided with the functionality of being able to detect an under-voltage condition in the input line voltage of the power supply so that the power supply can be shutdown gracefully without any

glitches on the output. In still another embodiment, the power supply controller is provided with the functionality of being able to detect an over-voltage condition in the input line voltage of the power supply so that the power supply can be shut down under this abnormal condition. This allows the power supply to handle much higher surge voltages due to the absence of reflected voltage and switching transients on the power switch in the power supply controller. In another embodiment, the power supply controller is provided with the functionality of being able to limit the maximum duty cycle of a switching waveform generated by a power supply controller to control the DC output of the power supply. In so doing, saturation of the transformer during power up is reduced and the excess power capability at high input voltages is safely limited. Increased duty cycle at low DC input voltages also allows for smaller input filter capacitance. Thus, this feature results in cost savings on many components in the power supply including the transformer. In yet another embodiment, some or all of the above functions are provided with a single multi-function terminal in the power supply controller. That is, in one embodiment, a plurality of additional functions are provided to power supply controller without the consequence of adding a corresponding plurality of additional terminals or pins to the integrated circuit package of the power supply controller. In one embodiment, one or some of the above functions are available when positive current flows into the multi-

function terminal. In another embodiment, one or some of the above functions are available when negative current flows out from the multi-function terminal. In one embodiment, the voltage at the multi-function terminal is fixed at a particular value depending on whether positive current flows into the multi-function terminal or whether negative current flows out from the multi-function terminal.

The multi-function features listed above not only save cost of many components and improve power supply performance but also, they save many components that would otherwise be required if these features were implemented externally.

Figure 1 is a block diagram illustrating one embodiment of a power supply 101 including a power supply controller 139 having a multi-function terminal 149 in accordance with the teachings of the present invention. As illustrated, power supply 101 includes an AC mains input 103, which is configured to receive an AC voltage input. A diode rectifier 105 is coupled to AC mains input to rectify the AC voltage. Capacitor 107 is coupled to diode rectifier 105 to convert the rectified AC into a steady DC line voltage 109, which is coupled to a primary winding 111 of a transformer. Zener diode 117 and diode 119 are coupled across primary winding 111 to provide clamp circuitry.

As illustrated in Figure 1, primary winding 111 is coupled to a drain terminal 141 of power supply controller 139. Power supply controller 139

includes a power switch 147 coupled between the drain terminal 141 and a source terminal 143, which is coupled to ground. When power switch 147 is turned on, current flows through primary winding 111 of the transformer. When current flows through primary winding 111, energy is stored in the transformer. When power switch 147 is turned off, current does not flow through primary winding 111 and the energy stored in the transformer is transferred to secondary winding 113 and bias winding 115.

A DC output voltage is produced at DC output 125 through diode 121 and capacitor 123. Zener diode 127, resistor 129 and opto-coupler 131 form feedback circuitry or regulator circuitry to produce a feedback signal received at a control terminal 145 of the power supply controller 139. The feedback or control signal is used to regulate or control the voltage at DC output 125. As the voltage across DC output 125 rises above a threshold voltage determined by Zener diode 127, resistor 129 and opto-coupler 131, additional feedback current flows into control terminal 145. In one embodiment, control terminal 145 also provides a supply voltage for circuitry of power supply controller 139 through bias winding 115, diode 133, capacitor 135 and capacitor 137.

As shown in Figure 1, power supply controller 139 includes a multi-function terminal 149, which in one embodiment enables power supply controller 139 to provide one or a plurality of different functions, depending on how multi-function terminal 149 is configured. Some

examples of how multi-function terminal 149 may be configured are shown in Figures 2A through 2F.

For instance, Figure 2A is a diagram illustrating one embodiment of a power supply controller 139 including a resistor 201 coupled between the multi-function terminal 149 and the source terminal 143. In one embodiment, the source terminal 143 is coupled to ground. In one embodiment, the voltage at multi-function terminal 149 is fixed when negative current flows from multi-function terminal 149. In one embodiment, the negative current that flows through resistor 201 is used to set externally the current limit of power switch 147. Thus, the power supply designer can choose a particular resistance for resistor 201 to set externally the current limit of power switch 147. In one embodiment, resistor 201 may be a variable resistor, a binary weighted chain of resistors or the like. In such embodiment, the current limit of power switch 147 may be adjusted externally by varying the resistance of resistor 201. In one embodiment, the current limit of power switch 147 is directly proportional to the negative current flowing through resistor 201.

Figure 2B is a diagram illustrating another embodiment of a power supply controller 139 including a switch 203 coupled between multi-function terminal 149 and source terminal 143. In one embodiment, source terminal 143 is coupled to ground. In one embodiment, power supply controller 139 switches power switch 147 when multi-function

terminal 149 is coupled to ground through switch 203. In one embodiment, power supply controller 139 does not switch power switch 147 when multi-function terminal 149 is disconnected from ground through switch 203. In particular, when an adequate amount of negative current flows from multi-function terminal 149, power supply 101 is enabled. When substantially no current flows from multi-function terminal 149, power supply 101 is disabled. In one embodiment, the amount of current that flows from multi-function terminal 149 to ground through switch 203 is limited. Thus, in one embodiment, even if multi-function terminal 149 is short-circuited to ground through switch 203, the amount of current flowing from multi-function terminal 149 to ground is limited to a safe amount.

Figure 2C is a diagram illustrating yet another embodiment of a power supply controller 139 including resistor 201 and switch 203 coupled in series between multi-function terminal 149 and source terminal 143, which in one embodiment is ground. The configuration illustrated in Figure 2C combines the functions illustrated and described in connection with Figures 2A and 2B above. That is, the configuration illustrated in Figure 2C illustrates a power supply controller 139 having external adjustment of the current limit of power switch 147, through the selection of the resistance for resistor 201, and on/off functionality through switch 203. When switch 203 is on, power supply controller 139 will switch

power switch 147 with a current limit set by resistor 201. When switch 203 is off, power supply controller 139 will not switch power switch 147 and power supply 101 will be disabled.

Figure 2D is a diagram illustrating still another embodiment of a power supply controller 139 including a resistor 205 coupled between the line voltage 109 and multi-function terminal 149. Referring briefly back to Figure 1 above, DC line voltage 109 is generated at capacitor 107 and is input to the primary winding 111 of the transformer of power supply 101. Referring back the Figure 2D, in one embodiment, multi-function terminal 149 is substantially fixed at a particular voltage when positive current flows into multi-function terminal 149. Therefore, the amount of positive current flowing through resistor 205 into multi-function terminal 149 is representative of line voltage 109, which is input to the primary winding 111. Since the positive current flowing through resistor 205 into multi-function terminal 149 represents the line voltage 109, power supply controller 139 can use this positive current to sense an under-voltage condition in line voltage 109 in one embodiment. An under-voltage condition exists when the line voltage 109 is below a particular under-voltage threshold value. In one embodiment, if a line under-voltage condition is detected, power switch 147 is not switched by power supply controller 139 until the under-voltage condition is removed.

In one embodiment, power supply controller 139 can use the

positive current flowing through resistor 205 into multi-function terminal 149 to detect an over-voltage condition in line voltage 109. An over-voltage condition when line voltage 109 rises above a particular over-voltage threshold value. In one embodiment, if a line over-voltage condition is detected, power switch 147 is not switched by power supply controller 139 until the over-voltage condition is removed.

In one embodiment, power supply controller 139 can also use the positive current flowing through resistor 205 and multi-function terminal 149 to detect for increases or decreases in line voltage 109. As line voltage 109 increases, for a given fixed maximum duty cycle, the maximum power available to secondary winding 113 in power supply 101 of Figure 1 usually increases. As line voltage 109 decreases, less power is available to secondary winding 113 in power supply 101. In most cases, the excess power available at the DC output 125 is undesirable under overload conditions due to high currents that need to be handled by components. In some instances, it is also desirable to increase the maximum power available to DC output 125 at low input DC voltages to save on cost of the input filter capacitor 107. Higher duty cycle at low DC input voltage allows lower input voltage operation for a given output power. This allows larger ripple voltage on capacitor 107, which translates to a lower value capacitor. Therefore, in one embodiment, power supply controller 139 adjusts the maximum duty cycle of a

switching waveform used to control or regulate power switch 147 in response to increases or decreases in line voltage 109. In one embodiment, the maximum duty cycle of the switching waveform used to control power switch 147 is inversely proportional to the line voltage 109. As mentioned earlier, reducing the duty cycle with increasing input DC voltage has many advantages. For instance, it reduces the value and hence the cost of capacitor 107. In addition, it limits excess power at high line voltages reducing the cost of the clamp circuit (117, 119), the transformer and the output rectifier 121 due to reduced maximum power ratings on these components.

It is appreciated that since only a single resistor 201 to ground, or a single resistor 205 to line voltage 109, is utilized for implementing some of the functions of power supply controller 139, a power savings is realized. For instance, if a resistor divider were to be coupled between power and ground, and a voltage output of the resistor divider coupled to a terminal of power supply controller 139 were to be used, current would continuously flow through both the resistor divider and into a sensor terminal of the power supply controller. This would result in increased power consumption. However in one embodiment of the power supply controller 139, only the single resistor 201 to ground or single resistor 205 to line voltage 109 is utilized, thereby eliminating the need for a current to flow through both the resistor divider and into power supply controller 139.

Figure 2E is a diagram illustrating yet another embodiment of a power supply controller 139 including resistor 205, as described above, coupled between the line voltage 109 and multi-function terminal 149. Figure 2E also includes a switch 207 coupled between control terminal 145 and multi-function terminal 149. In one embodiment, resistor 205 provides the same functionality as discussed above in connection with Figure 2D. Therefore, when switch 207 is switched off, the configuration illustrated in Figure 2E is identical to the configuration described above in connection with Figure 2D.

In one embodiment, control terminal 145 provides a supply voltage for power supply controller 139 in addition to providing a feedback or control signal to power supply controller 139 from DC output 125. As a result, in one embodiment, switch 207 provides in effect a switchable low resistance connection between a supply voltage (control terminal 145) and multi-function terminal 149. In one embodiment, the maximum positive current that can flow into multi-function terminal 149 is limited. Therefore, in one embodiment, even when switch 207 provides, in effect, a short-circuit connection from a supply voltage, the positive current that flows into multi-function terminal 149 is limited to a safe amount. However, in one embodiment, the positive current that does flow through switch 207, when activated, into multi-function terminal 149 triggers an over-voltage condition. As discussed above, power supply 139

discontinues switching power switch 147 during an over-voltage condition until the condition is removed. Therefore, switch 207 provides on/off functionality for power supply controller 139. When switch 207 is the activated, the low resistance path to control terminal 145 is removed and the positive current flowing into multi-function terminal 149 is limited to the current that flows from line voltage 109 through resistor 205. Assuming that neither an under-voltage condition nor an over-voltage condition exists, power supply controller 139 will resume switching power switch 147, thereby re-enabling power supply 101.

Figure 2F is a diagram illustrating another embodiment of a power supply controller 139 using current mode control to regulate the current limit of the power supply. As shown, resistor 201 is coupled between the multi-function terminal 149 and the source terminal 143 and the transistor 209 of an opto-coupler coupled between multi-function terminal 149 and a bias supply, such as for example control terminal 145. Similar to Figure 2A, the negative current that flows out from multi-function terminal 149 is used to set externally the current limit of power switch 147. In the embodiment illustrated in Figure in Figure 2F, the current limit adjustment function can be used for controlling the power supply output by feeding a feedback signal from the output of the power supply into multi-function terminal 149. In the embodiment depicted in Figure 2F, the current limit is adjusted in a closed loop to regulate the output of the power supply

(known as current mode control) by adding the opto-coupler output between multi-function terminal 149 and the bias supply.

In one embodiment, the power supply controller configurations described in connection with Figures 2A through 2F all utilize the same multi-function terminal 149. Stated differently, in one embodiment, the same power supply controller 139 may be utilized in all of the configurations described. Thus, the presently described power controller 139 provides a power supply designer with added flexibility. As a result, a power supply designer may implement more than one of the above functions at the same time using the presently described power supply controller 139. In addition, the same functionality may be implemented in more than one way. For example, power supply 101 can be remotely turned on and off using either power or ground. In particular, the power supply 101 can be turned on and off by switching to and from the control terminal (supply terminal for the power supply controller) using the over-voltage detection feature, or by switching to and from ground using the on/off circuitry.

Figures 2A though 2F provide just a few examples of use of the multi-function terminal. A person skilled in the art will find many other configurations for use of the multifunction pin. The uses for the multi-function terminal, are therefore, not limited to the few examples shown.

It is worthwhile to note that different functions of the presently

described power supply controller 139 may be utilized at different times during different modes of operation of power supply controller 139. For instance, some features may be implemented during startup operation, other functions may be implemented during normal operation, other functions may be implemented during fault conditions, while still other functions may be implemented during standby operation. Indeed, it is appreciated that a power supply designer may implement other circuit configurations to use with a power supply controller 139 in accordance with teachings of the present invention. The configurations illustrated in Figures 2A through 2F are provided simply for explanation purposes.

Figure 3 is a block diagram illustrating one embodiment of a power supply controller 139 in accordance with teachings of the present invention. As shown in the embodiment illustrated, power supply controller 139 includes a current input circuit 302, which in one embodiment serves as multi-function circuitry. In one embodiment, current input circuit 302 includes a negative current input circuit 304 and a positive current input circuit 306. In one embodiment, negative current input circuit 304 includes negative current sensor 301, on/off circuitry 309 and external current limit adjuster 313. In one embodiment, positive current input circuit 306 includes positive current sensor 305, under-voltage comparator 317, over-voltage comparator 321 and maximum duty cycle adjuster 325.

As shown in Figure 3, negative current sensor 301 and positive current sensor 305 are coupled to multi-function terminal 149. In one embodiment, negative current sensor 301 generates a negative current sense signal 303 and positive current sensor generates a positive current sense signal 307. For purposes of this description, a negative current may be interpreted as current that flows out of multi-function terminal 149. Positive current may be interpreted as current that flows into multi-function terminal 149. In one embodiment, on/off circuitry 309 is coupled to receive negative current sense signal 303. External current limit adjuster 313 is coupled to receive negative current sense signal 303.

In one embodiment, under-voltage comparator 317 is coupled to receive positive current sense signal 307. Over-voltage comparator 321 is coupled to receive positive current sense signal 307. As discussed earlier, both under-voltage and over-voltage comparators also function as on/off circuits. Maximum duty cycle adjuster 325 is also coupled to receive positive current sense signal 307.

In one embodiment, on/off circuitry 309 generates an on/off signal 311, under-voltage comparator 317 generates an under-voltage signal 319 an over-voltage comparator 321 generates an over-voltage signal 323. As shown in the embodiment illustrated in Figure 3, enable/disable logic 329 is coupled to receive the on/off signal 311, the under-voltage signal 319 and the over-voltage signal 323. The under-voltage and over-

voltage signals can also be used for on/off functions as noted earlier.

In one embodiment, enable/disable logic 329 generates an enable/disable signal 331, which is coupled to be received by control circuit 333. The control circuit 333 is also coupled to receive a control signal from control terminal 145. In addition, control circuit 333 is also coupled to receive a drain signal from drain terminal 141, a maximum duty cycle adjustment signal 327 from maximum duty cycle adjuster 325 and an external current limit adjustment signal 315 from external current limit adjuster 313.

In one embodiment, control circuit 333 generates a switching waveforms 335, which is coupled to be received by power switch 147. In one embodiment, power switch 147 is coupled between drain terminal 141 and source terminal 143 to control a current flowing through the primary winding 111 of power supply 101, which is coupled to drain terminal 141.

In one embodiment, negative current sensor 301 senses current that flows out of negative current sensor 301 through multi-function terminal 149. Negative current sense signal 303 is generated in response to the current that flows from negative current sensor 301 through multi-function terminal 149. In one embodiment, current that flows from negative current sensor 301 through multi-function terminal 149 typically flows through an external resistance or switch coupled between multi-function terminal 149 and ground.

In one embodiment, positive current sensor 305 senses current that flows into positive current sensor 305 through multi-function terminal 149. Positive current sense signal 307 is generated in response to the current that flows into positive current sensor 305 through multi-function terminal 149. In one embodiment, current that flows into positive current sensor 305 through multi-function terminal 149 typically flows through an external resistance coupled between multi-function terminal 149 and the DC line voltage 109 input to the primary winding 111 of a power supply 101 and/or another voltage source. In another embodiment the current flows through an external resistance or a switch coupled between the multi-function terminal 149 and another voltage source. In one embodiment, the line voltage 109 input to primary winding 111 is typically a rectified and filtered AC mains signal.

As mentioned above, in one embodiment, positive current does not flow while negative current flows, and vice versa. In one embodiment, the negative current sensor 301 and positive current sensor 305 are designed in such a way that they are not active at the same time . Stated differently, negative current sense signal 303 is not active at the same time as positive current sense signal 307 in one embodiment.

In one embodiment, the voltage at multi-function terminal 149 is fixed at a first level when negative current flows out of power supply controller 139 from multi-function terminal 149. In one embodiment, the

first level is selected to be approximately 1.25 volts. In one embodiment, the voltage at multi-function terminal is fixed at a second level when positive current flows into power supply controller 139 through multi-function terminal 149. In one embodiment, the second level is selected to be approximately 2.3 volts.

In one embodiment, on/off circuitry 309 generates on/off signal 311 in response to negative current sense signal 303. In one embodiment, when the current flowing from multi-function terminal 149 through an external resistance to ground is less than a predetermined on/off threshold level, on/off circuitry 309 generates on/off signal 311 to switch off the power supply 101. In one embodiment, when the current flowing from multi-function terminal 149 is greater than a predetermined on/off threshold level, on/off circuitry 309 generates on/off signal 311 to switch on the power supply 101. In one embodiment, the magnitude of the on/off threshold level is approximately 40 to 50 microamps, including hysteresis.

In one embodiment, external current limit adjuster 313 generates external current limit adjustment signal 315 in response to negative current sense signal 303. In one embodiment, when the magnitude of the negative current flowing from multi-function terminal 149 through an external resistance or switch to ground is below a predetermined level, the current limit adjuster 313 generates an external current limit adjustment signal to limit the current flowing through power switch 147. In one

embodiment, when the magnitude of the negative current flowing from multi-function terminal 149 is below a predetermined level, the current flowing through power switch 147 is limited to an amount directly proportional to the current flowing out of power supply controller 139 from multi-function terminal 149. In one embodiment, predetermined level is approximately 150 microamps. In one embodiment, if the magnitude of the negative current flowing out of power supply controller 139 from multi-function terminal 149 is greater than the predetermined level, the current flowing through power switch 147 is internally limited or clamped to a fixed safe maximum level. Therefore, the current flowing through power switch 147 is clamped to a safe value, even when multi-function terminal 149 is shorted to ground. In one embodiment, the current flowing through power switch 147 is internally limited or clamped to value of 3 amps.

In one embodiment, since the voltage at multi-function terminal 149 is fixed at a particular voltage when current flows out of power supply controller 139 through multi-function terminal 149, the current limit through power switch 147 can be accurately set externally with a single large value, low-cost, resistor externally coupled between multi-function terminal 149 and ground. By using a large external resistance, the current flowing from multi-function terminal 149 is relatively small. As mentioned above, the current flowing from multi-function terminal 149 in one embodiment is in the microamp range. Since the current flowing from multi-function

terminal 149 is relatively small, the amount of power dissipated is also relatively small.

In one embodiment, multi-function terminal 149 is coupled to the DC line voltage 109 input to the primary winding 111 through an external resistance. In one embodiment, the amount of current flowing into multi-function terminal 149 represents the DC input line voltage to the power supply 101. In one embodiment, under-voltage comparator 317 generates under-voltage signal 319 in response to the resulting positive current sense signal 307. In one embodiment, when the current flowing into multi-function terminal 149 rises above a first predetermined threshold, under-voltage comparator 317 generates under-voltage signal 319 to enable the power supply. In one embodiment, when the current flowing into multi-function terminal 149 falls below a second predetermined threshold, under-voltage comparator 317 generates under-voltage signal 319 to disable the power supply. In one embodiment, the first predetermined threshold is greater than the second predetermined threshold to provide hysteresis. By providing hysteresis or a hysteretic threshold, unwanted switching on and off of the power supply 101 resulting from noise or ripple is reduced. In one embodiment, the first predetermined threshold is approximately 50 microamps and the second predetermined threshold is approximately 0 microamps. In another embodiment, a hysteretic threshold is not utilized. Thus the hysteresis is

greater than or equal to zero.

In one embodiment, over-voltage comparator 321 generates over-voltage signal 323 in response to the positive current sense signal 307. In one embodiment, when the current flowing into multi-function terminal 149 rises above a third predetermined threshold, over-voltage comparator 321 generates over-voltage signal 323 to disable the power supply. In one embodiment, when the current flowing into multi-function terminal 149 falls below a fourth predetermined threshold, over-voltage comparator 321 generates over-voltage signal 323 to enable the power supply. In one embodiment, the third predetermined threshold is greater than the fourth predetermined threshold to provide hysteresis. By providing hysteresis or a hysteretic threshold, unwanted switching on and off of the power supply resulting from noise is reduced. In one embodiment, the third predetermined threshold is approximately 225 microamps and the fourth predetermined threshold is approximately 215 microamps. In one embodiment, the third and fourth predetermined thresholds are selected to be approximately four to five times greater than the first predetermined threshold discussed above for an AC mains input 103 of approximately 85 volts to 265 volts AC. In another embodiment, a hysteretic threshold is not utilized. Thus the hysteresis is greater than or equal to zero.

In one embodiment, power switch 147 is able to tolerate higher voltages when not switching. When the power supply is disabled, power

switch 147 does not switch. Therefore, it is appreciated that over-voltage comparator 321 helps to protect the power supply 101 from unwanted input power surges by disabling the power switch 147.

In one embodiment, over-voltage and under-voltage comparators 321 and 317 may also be used for on/off functionality, similar to on/off circuitry 309. In particular, multi-function terminal 149 may be switchably coupled to a on/off control signal source to provide a positive current that flows into multi-function terminal 149 that cross the under-voltage or over-voltage thresholds (going above the third or below the fourth predetermined thresholds). For example, when the positive current through the multifunction pin crosses above the first predetermined threshold of the under-voltage comparator 317, the power supply will be enabled and when the positive current goes below the second predetermined threshold of the under-voltage comparator 317, the power supply is disabled. Similarly, when the positive current through the multifunction pin crosses above the third predetermined threshold of the over-voltage comparator 321, the power supply will be disabled and when the positive current goes below the fourth predetermined threshold of the over-voltage comparator 321, the power supply is enabled.

In one embodiment, maximum duty cycle adjuster 325 generates maximum duty cycle adjustment signal 327 in response to the positive current sense signal 307. In one embodiment, maximum duty cycle

adjustment signal 327, which is received by control circuit 333, is used to adjust the maximum duty cycle of the switching waveform 335 used to control power switch 147. In one embodiment, the maximum duty cycle determines how long a power switch 147 can be on during each cycle. For example, if the maximum duty cycle is 50 percent, the power switch 147 can be on for a maximum of 50 percent of each cycle.

Referring briefly for example to the power supply 101 of Figure 1, while power switch 147 is on, power is stored in the transformer core through the primary winding 111. While the power switch 147 is off, power is delivered from the transformer core to the secondary winding of the transformer in power supply 101. To delivery a given power level, for a lower DC input voltage 109, a higher duty cycle is required and for a higher DC input voltage 109, a lower duty cycle is required. In one embodiment of the present invention, maximum duty cycle adjuster 325 decreases the maximum duty cycle of power switch 147 in response to increases in the DC input voltage 109. In one embodiment, maximum duty cycle adjuster 325 increases the maximum duty cycle of power switch 147 in response to decreases in the DC input voltage 109. Stated differently, the maximum duty cycle is adjusted to be inversely proportional to the current that flows into multi-function terminal 149 in one embodiment of the present invention.

Referring back to Figure 3, in one embodiment, the maximum duty

cycle is adjusted within a range of 33 percent to 75 percent based on the amount of positive current that flows into multi-function terminal 149. In one embodiment, maximum duty cycle adjuster 325 does not begin to decrease the maximum duty cycle until the amount of current that flows into multi-function terminal 149 rises above a threshold value. In one embodiment, that threshold value is approximately 60 microamps. In one embodiment, the maximum duty cycle is not adjusted if negative current flows out of multi-function terminal 149. In this case, the maximum duty cycle is fixed at 75 percent in one embodiment of the present invention.

In one embodiment, enable/disable logic 329 receives as input on/off signal 311, under-voltage signal 319 and over-voltage signal 323. In one embodiment, if any one of the under-voltage or over-voltage conditions exist, enable/disable logic 329 disables power supply 101. In one embodiment, when the under-voltage and over-voltage conditions are removed, enable/disable logic 329 enables power supply 101. In one embodiment, power supply 101 may be enabled or disabled by starting and stopping, respectively, the switching waveform 335 at the beginning of a switching cycle just before the power switch is to be turned on. In one embodiment, enable/disable logic 329 generates enable/disable signal 331, which is received by the oscillator in the control circuit 333 to start or stop the oscillator at the beginning of a switching cycle of switching waveform 335. When enabled the oscillator will start a new on

cycle of the switching waveform. When disabled the oscillator will complete the current switching cycle and stop just before the beginning of the next cycle.

In one embodiment, control circuit 333 generates switching waveform 335 to control power switch 147 in response to a current sense signal received from drain terminal 141, enable/disable signal 331, maximum duty cycle adjustment signal 327, a control signal from control terminal 145 and external current limit adjustment signal 315.

In one embodiment, the enable/disable signal can also be used to synchronize the oscillator in the control circuit to an external on/off control signal source having a frequency less than that of the oscillator. The on/off control signal can be input to the multi-function terminal through any of the three paths that generate the enable/disable signal: on/off circuitry 309, under-voltage comparator 317 or over-voltage comparator 321. As discussed, enable/disable the oscillator in the control circuit 333, in one embodiment, begins a new complete cycle of switching waveform at 335 using known techniques in response to enable/disable signal 331, which represents the on/off control signal at the multi-function input. By turning the on/off control signal "on" at the multi-function input for a fraction of the switching cycle and then "off," the oscillator is enabled to start a new complete cycle. Therefore, if the external on/off control signal has short "on" pulses at a frequency less than the oscillator in the control circuit, the

oscillator will produce a switching cycle each time an on pulse is detected, thus providing a switching waveform that is synchronized to the external frequency.

In an alternate embodiment shown below in Figure 7, the enable/disable signal 331 directly disables or turns off the power switch through the AND gate 493 when an under-voltage or over-voltage condition exists. In this embodiment, the power switch can be enabled or disabled in the middle of a cycle and consequently, synchronization of the switching waveform through a on/off control signal at the multi-function input is not provided.

Figure 4 is a schematic of one embodiment of a power supply controller 139 in accordance with the teachings of the present invention. As illustrated, negative current sensor 301 includes a current source 401 coupled to control terminal 145. Transistors 403 and 405 form a current mirror coupled to current source 401. In particular, transistor 403 has a source coupled to current source 401 and a gate and drain coupled to the gate of transistor 405. The source of transistor 405 is also coupled to current source 401. Transistor 407 is coupled between the drain and gate of transistor 403 and multi-function terminal 149. In one embodiment, the gate of transistor 407 is coupled to a band gap voltage V_{BG} plus a threshold voltage V_{TN}. In one embodiment, V_{BG} is approximately 1.25 volts, V_{TN} is approximately 1.05 volts and $V_{BG} + V_{TN}$ is approximately 2.3

volts. Transistors 411 and 413 also form a current mirror coupled to the drain of transistor 405. In particular, the gate and drain of transistor 411 are coupled to the drain of transistor 405 and the gate of transistor 413. In one embodiment, negative current sense signal 303 is generated at the gate and drain of transistor 411. The sources of transistors 411 and 413 are coupled to ground. In one embodiment, ground is provided through source terminal 143.

In one embodiment, on/off circuitry 309 includes a current source 409 coupled between the drain of transistor 413 and control terminal 145. In one embodiment, on/off signal 311 is generated at the drain of transistor 413.

In one embodiment, external current limit adjuster 313 includes a current source 415 coupled between control terminal 145 and the drain of transistor 419 and the gate and drain of transistor 421. The source of transistor 419 and the source of transistor 421 are coupled to ground. The gate of transistor 419 is coupled to receive negative current sense signal 303. External current limit adjuster 313 also includes a current source 417 coupled between control terminal 145 and the drain of transistor 423 and resistor 425. The source of transistor 423 and resistor 425 are coupled to ground. External current limit adjustment signal 315 is generated at the drain of transistor 423.

In one embodiment, positive current sensor 305 includes transistor

429 having a source coupled to multi-function terminal 149 and the current mirror formed with transistors 431 and 433. In particular, transistor 431 has a gate and drain coupled to the drain of transistor 429 and the gate of transistor 433. Current source 435 is coupled between ground and the sources of transistors 431 and 433. The gate of transistor 429 is coupled to band gap voltage V_{BG}. The drain of transistor 433 is coupled to the current mirror formed with transistors 427 and 437. In particular, the gate and drain of transistor 427 are coupled to the gate of transistor 437 and the drain of transistor 433. The sources of transistors 427 and 437 are coupled to control terminal 145. Positive current sense signal 307 is generated at the gate and drain of transistor 427.

In one embodiment, under-voltage comparator 317 includes a current source 439 coupled between the drain of transistor 437 and ground. Under-voltage signal 319 is generated at the drain of transistor 437.

In one embodiment, over-voltage comparator 321 includes a current source 443 coupled between the drain of transistor 441 and ground. Transistor 441 has a source coupled to control terminal 145 and a gate coupled to receive positive current sense signal 307. Over-voltage signal 323 is generated at the drain of transistor 441.

In one embodiment, enable/disable logic 329 includes NOR gate 445 having an input coupled to receive under-voltage signal 319 and an

inverted input coupled to receive on/off signal 311. Enable/disable logic 329 also includes NOR gate 447 having an input coupled to receive over-voltage signal 323 and an input coupled to an output of NOR gate 445. Enable/disable signal 331 is generated at the output of NOR gate 447.

In one embodiment, maximum duty cycle adjuster 325 includes a transistor 449 having a source coupled to control terminal 145 and a gate coupled to receive positive current sense signal 307. Maximum duty cycle adjuster 325 also includes a current source 453 coupled between the drain of transistor 449 and ground. A diode 451 is coupled to the drain of transistor 449 to produce maximum duty cycle adjustment signal 327.

In one embodiment, power switch 147 includes a power metal oxide semiconductor field effect transistor (MOSFET) 495 coupled between drain terminal 141 and source terminal 143. Power MOSFET 495 has a gate coupled to receive a switching waveform 335 generated by pulse width modulator 333.

In one embodiment, control circuit 333 includes a resistor 455 coupled to the control terminal 145. A transistor 457 has a source coupled to resistor 455 and a negative input of a comparator 459. A positive input of comparator 459 is coupled to a voltage V, which in one embodiment is approximately 5.7 volts. An output of comparator 459 is coupled to the gate of transistor 457. The drain of transistor 457 is coupled to diode 451 and resistor 479. The other end resistor 479 is

coupled to ground. A filter is coupled across resistor 479. The filter includes a resistor 481 coupled to resistor 479 and capacitor 483 coupled to resistor 481 and ground. Capacitor 483 is coupled to a positive input of comparator 477.

In one embodiment, control circuit 333 is a pulse width modulator, which has an oscillator 467 with three oscillating waveform outputs 471, 473 and 475. Oscillator 467 also includes an enable/disable input 469 coupled to receive enable/disable signal 331. In one embodiment, control circuit 333 also includes a voltage divider including resistors 461 and 463 coupled between drain terminal 141 and ground. A node between resistors 461 and 463 is coupled to a positive input of a comparator 465. A negative input of comparator 465 is coupled to receive external current limit adjustment signal 315.

In one embodiment, oscillating waveform output 471 is coupled to a first input of AND gate 493. Oscillating waveform output 473 is coupled to a set input of latch 491. Oscillating waveform output 475 is coupled to a negative input of comparator 477. An output of comparator 465 is coupled to a first input of AND gate 487. A leading edge blanking delay circuit 485 is coupled between the output of NAND gate 493 and a second input of AND gate 487. In one embodiment, there is a gate driver or a buffer between the output of the NAND gate 493 and the gate of the MOSFET (not shown). An output of AND gate 487 is coupled to a first

input of OR gate 489. A second input of OR gate 489 is coupled to an output of comparator 477. An output of OR gate 489 is coupled to a reset input of latch 491. An output of latch 491 is coupled to a second input of AND gate 493. The output of AND gate 493 generates switching waveform 335.

Operation of power supply controller 139 of Figure 4 is as follows. Beginning with negative current sensor 301, the gate of transistor 407 is fixed at $V_{BG} + V_{TN}$ in one embodiment to approximately 2.3 volts. As a result, transistor 407 sets the voltage at multi-function terminal 149 to V_{BG} in one embodiment, which is approximately 1.25 volts, when current is pulled out of multi-function terminal 149. This current may be referred to as negative current since the current is being pulled out of power supply controller 139. In one embodiment, transistor 407 is sized such that it operates with a current density resulting in a voltage drop between the gate and source that is close to V_{TN}, wherein the V_{TN} is the threshold of the N channel transistor 407, when negative current flows from multi-function terminal 149.

When an external resistor (not shown) is coupled from multi-function terminal 149 to ground, the negative current flowing through the external resistor will therefore be V_{BG} divided by the value of the external resistor in accordance with Ohm's law. This negative current flowing out from multi-function terminal 149 passes through transistors 403 and is

mirrored on to transistor 405. Current source 401 limits the negative current sourced by multi-function terminal 149. Therefore, even if multi-function terminal 149 is short-circuited to ground, the current is limited to a current less than the current supplied by current source 401. This current is less than the current source 401 by an amount that flows through the transistor 405. In one embodiment, the negative current that can be drawn from the multi-function terminal is limited to 200 microamps by the current source 401. In one embodiment, if more negative current than current source 401 is able to supply is pulled from multi-function terminal 149, the voltage at multi-function terminal 149 collapses to approximately 0 volts.

The current that flows through transistor 403 is mirrored to transistor 405. The current that flows through transistors 405 and 411 is the same since they are coupled in series. Since transistors 411 and 413 form a current mirror, the current flowing through transistor 413 is proportional to the negative current flowing through multi-function terminal 149. The current flowing through transistor 413 is compared to the current provided by current source 409. If the current through transistor 413 is greater than the current supplied by current source 409, the signal at the drain of transistor 413 will go low, which in one embodiment enables the power supply. Indeed, on/off signal 311 is received at an inverted input of NOR gate 445. Thus, when on/off signal 311 is low, the

power supply is enabled. Therefore, by having a negative current greater than a particular threshold value, the power supply of the present invention is enabled in one embodiment. In one embodiment, the magnitude of that particular threshold value is approximately 50 microamps.

As mentioned above, the current flowing through transistor 411 is proportional to the negative current flowing out from multi-function terminal 149. As illustrated, transistor 419 also forms a current mirror with transistor 411. Therefore, the current flowing through transistor 419 is proportional to the current flowing through transistor 411. The current flowing through transistor 421 is the difference between the current supplied by current source 415 and the current flowing through transistor 419. For example, assume that the current supplied by current source 415 is equal to A. Assume further that the current flowing through transistor 419 is equal to B. In this case, the current flowing through transistor 421 is equal to A - B.

As illustrated, transistor 423 forms a current mirror with transistor 421. Therefore, the current flowing through transistor 423 is proportional to the current flowing through transistor 421. Continuing with the example above and assuming further that transistors 421 and 423 are equal in size, the current flowing through transistor 423 is also equal to A - B. Assuming further that current source 417 supplies a current equal to the

current supplied by current source 415, which is assumed to be equal to A, then the current flowing through resistor 425 would be equal to A - (A - B), which is equal to B.

Therefore, the current flowing through resistor 425 is proportional to the current flowing through transistor 419, which is proportional to the current flowing through transistor 411, which is proportional to the negative current flowing out from multi-function terminal 149. Note that if the current flowing through transistor 419 is greater than the current supplied by current source 415, the current flowing through transistor 421 would be zero because the voltage at the drains of transistors 419 and 421 would collapse to approximately zero volts. This would result in the current flowing through transistor 423 to be zero . Thus, the current through resistor 425 cannot be greater than the current supplied by current source 417. However, as long as B is less than A, the current that flows through resistor 425 is equal to B. If B rises above A, the current that flows through resistor 425 is equal to A.

In one embodiment, resistor 425 is fabricated using the same or similar types of processes and diffusions or doped regions used in fabricating power MOSFET 495. As a result, the on resistance of resistor 425 follows or tracks the on resistance of power MOSFET 495 through varying operating conditions and processing variations.

The voltage across resistor 425 is reflected in external current limit

adjuster signal 315, which is input to the negative input of comparator 465. In one embodiment, the negative input of comparator 465 is the threshold input of comparator 465. Therefore, the negative input of comparator 465 receives a voltage proportional to the negative current flowing out of multi-function terminal 149 multiplied by the resistance of resistor 425.

The positive input of comparator 465 is coupled to drain terminal 141 through resistor 461 of the voltage divider formed by resistor 461 and resistor 463. Therefore, the positive input of comparator 465 senses a voltage proportional to the drain current of power MOSFET 495 multiplied by the on resistance of power MOSFET 495.

When the voltage at the positive terminal of comparator 465 rises above the voltage provided by external current limit adjuster signal 315 to the negative terminal of comparator 465, the output of comparator 465 is configured to reset latch 491 through AND gate 487 and OR gate 489. By resetting latch 491, the on portion of a cycle of waveform 335 received at the gate of power MOSFET 495 is masked or cut short, which results in turning off power MOSFET 495 when the amount of current flowing through power switch 147 rises above the threshold.

In one embodiment, AND gate 487 also receives input from leading edge blanking delay circuitry 485. In one embodiment, leading edge blanking delay circuitry 485, using known techniques, temporarily disables

current limit detection at the start, or during the leading edge portion, of an on transition of power MOSFET 495.

As shown in the embodiment illustrated in Figure 4, latch 491 is set at the beginning of each cycle by switching waveform output 473. One way that latch 491 is reset, thereby turning off power MOSFET 495, is through the output of comparator 465. Another way to reset latch 491 is through the output of comparator 477, which will be discussed below in connection with maximum duty cycle adjuster 325.

With regard to positive current sensor 305, the gate of transistor 429 is coupled to the band gap voltage V_{BG}. In one embodiment, transistor 429 is sized such that it operates with a current density resulting in a drop between the source and gate close to $V_{TP,}$ which is threshold of the P channel transistor 429, when positive current flows into multi-function terminal 149. In one embodiment, current that flows into multi-function terminal 149 is referred to as positive current since the current is being fed into the power supply controller 139. As a result, the voltage at multi-function terminal 149 is fixed at approximately $V_{BG} + V_{TP}$ when positive current flows into multi-function terminal 149.

The gate voltages on the transistors 407 and 429 chosen in the embodiment discussed above are such that only one of transistors 407 and 429 are switched on at a time depending on the polarity of the current at the multi-function terminal. Stated differently, if transistor 407 is on,

transistor 429 is off. If transistor 429 is on, transistor 407 is off. As result, if negative current sensor 301 is on, positive current sensor 305 is isolated from multi-function terminal 149. If positive current sensor 305 is on, negative current sensor 301 is isolated from multi-function terminal 149. Therefore, if there is negative current flowing through multi-function terminal 149, positive current sensor 305 is disabled. If there is positive current flowing through multi-function terminal 149, negative current sensor 301 is disabled.

In one embodiment, the positive current that flows into transistor 429 flows through transistor 431 since they are coupled in series. The positive current through multi-function terminal 149 flows into and is limited by current source 435. In one embodiment, if the positive current through multi-function terminal 149 is greater than an amount that current source 435 can sink minus the current in transistor 433, then the voltage at multi-function terminal 149 will rise and is clamped either by the circuitry driving the current or by the standard clamping circuitry that is used for protection purposes on external terminals such as the multi-function terminal, of a power supply controller. As shown, transistors 431 and 433 form a current mirror. Therefore, the current flowing through transistor 433 is proportional to the positive current that flows through transistor 431. The current that flows through the transistor 433 flows to transistor 427 since they are coupled in series. As shown, the gate of transistor 427 is

coupled to the drain of transistor 427, which generates positive current sense signal 307.

Transistors 427 and 437 form a current mirror since the gate and drain of transistor 427 are coupled to the gate of transistor 437. Therefore, the current flowing through transistor 437 is proportional to the current flowing through transistor 427, which is proportional to the positive current. Current source 439 provides a reference current, which is compared to the current that flows through transistor 437. If the current flowing through transistor 437 rises above the current provided by current source 439, then the voltage at the drain of transistor 437, which is the under-voltage signal 319, goes high. When under-voltage signal 319 goes high and the output of NOR gate 445 will go low, indicating that there is no under-voltage condition.

Transistors 427 and 441 also form a current mirror since the gate and drain of transistor 427 are coupled to the gate of transistor 441. Therefore, the current flowing through transistor 441 is proportional to the current flowing through the transistor 427, which is proportional to the positive current. Current source 443 provides a reference current, which is compared to current that flows through transistor 441. As long as the current flowing through transistor 441 stays below the current provided by current source 443, then the voltage at the drain of transistor 441, which is the over-voltage signal 323, remains low. When over-voltage signal 323

remains low, the output of NOR gate 447 remains high assuming that there was no under-voltage condition indicated by under-voltage signal 319 and no remote off condition indicated by on/off signal 311.

The output of NOR gate 447 is enable/disable signal 331. In one embodiment, enable/disable signal 331 is high if on/off signal 311 is low, or under-voltage signal 319 is high and over-voltage signal 323 is low. Otherwise, enable/disable signal 331 is low.

In one embodiment, the oscillator 467 receives enable/disable signal 331 at the start/stop input 469. In one embodiment, oscillator 467 generates oscillating waveforms at oscillating waveform outputs 471, 473 and 475 while enable/disable signal 331 is high or active. In one embodiment, oscillator 467 does not generate the oscillating waveforms at oscillating waveform outputs 471, 473 and 475 while enable/disable signal 331 is low or in-active. In one embodiment, oscillator 467 begins generating oscillating waveforms starting with new complete cycles on a rising edge of enable/disable signal 331. In one embodiment, oscillator 467 completes existing cycles of the oscillating waveforms generated at oscillating waveform outputs 471, 473 and 475 before stopping the waveforms in response to a falling edge of enable/disable signal 331. That is, oscillator 467 stops generating the waveforms at a point just before the start of an on time of power switch of the next cycle in response to a falling edge of enable/disable signal 331.

In one embodiment, control terminal 145 supplies power to the circuitry of power supply controller 139 and also provides feedback to modulate the duty cycle of switching waveform 335. In one embodiment, control terminal 145 is coupled to the output of the power supply 101 through a feedback circuit to regulate the output voltage of the power supply 101. In one embodiment, an increase in the output voltage of power supply 101 results in the reduction in the duty cycle of switching waveform 335 through feedback received through control terminal 145. Therefore, if the regulation level of the output parameter of power supply 101 that is being controlled, such as output voltage or current or power, is exceeded during operation, additional feedback current is received through control terminal 145. This feedback current flows through resistor 455 and through a shunt regulator formed by transistor 457 and comparator 459. If no feedback current or control terminal current in excess of supply current is received through control terminal 145, the current through transistor 457 is zero. If the current through transistor 457 is zero, and assuming for the time being that there is no current through the diode 451, the current through resistor 479 is zero. If there is no current flowing through resistor 479, then the voltage drop across resistor 479 is zero. If there is no voltage drop across resistor 479, there is no voltage drop across capacitor 483. As a result, the output of comparator 477 will remain low. If the output of comparator 477 remains low, and

assuming for the time being that the output of AND gate 487 remains low, the output of latch 491 will remain high. In this case, the maximum duty cycle signal, which is produced by oscillator waveform output 471, will be generated at the output of AND gate 493. Thus, switching waveform 335 will have the maximum duty cycle produced by oscillator waveform output 471.

Therefore, when the voltage drop across resistor 479 remains at zero, the maximum duty cycle produced at oscillator waveform output 471 is not limited, assuming that the output of AND gate 487 remains low. This is because latch 491 is not reset through the output of comparator 477. However, when the feedback current or control terminal current in excess to the supply current is received through control terminal 145, this feedback current flows through transistor 457. As the amount of current flowing through the transistor 457 increases, the voltage drop across resistor 479 increases correspondingly. As a voltage drop across resistor 479 increases, the voltage drop across capacitor 483 will increase. In any given cycle, when the voltage on the oscillating waveform output 475 crosses below the voltage across the capacitor 483 the output of the comparator will go high and terminate the on-time of the switching waveform 335 or turn off the power switch 495. As a result, the duty cycle (on time as a fraction of the cycle time) of the switching waveform 335 decreases with increase in voltage drop across resistor 479.

In one embodiment, the oscillating waveform at oscillating waveform output 475 is a sawtooth waveform having a duty cycle and period equal to the maximum duty cycle waveform generated at oscillating waveform output 471. As the voltage drop across resistor 479 increases, the output of comparator 477 will go high closer to the beginning of each cycle. When the output of comparator 477 goes high, latch 491 will be reset through NOR gate 489. When latch 491 is reset, the on time of the of switching waveform 335 is terminated for that particular cycle and switching waveform 335 remains low for the remainder of that particular cycle. Latch 491 will not be set again until the beginning of the next cycle through switching waveform output 473, assuming that there is a high or active enable/disable signal 331.

Referring now to maximum duty cycle adjuster signal 325, transistor 449 includes a source coupled to control terminal 145 and a gate coupled the gate and drain of transistor 427 to receive positive current sense signal 307. Transistor 449 and transistor 427 also form a current mirror. Therefore, the current flowing through transistor 449 is proportional to the current flowing through transistor 427, which is proportional to the positive current flowing into multi-function terminal 149. The current that flows through diode 451 is the difference between the current that flows through transistor 449 and the current that flows into current source 453. The current that flows through current source 453 is

set such that current will not begin to flow through diode 451 until the current flowing through transistor 449 rises above a threshold. In one embodiment, the above threshold value is chosen such that the maximum duty cycle is not reduced until the positive current flowing into multi-function terminal 149 rises above the threshold used for under-voltage comparison. In one embodiment, the threshold positive current used for under-voltage comparison is approximately 50 microamps and the threshold positive current used for maximum duty cycle adjustment is approximately 60 microamps.

When current begins to flows through diode 451, that current will be combined with current that flows through transistor 457. In one embodiment, the current that flows through diode 451 is maximum duty cycle adjustment signal 327. The current flowing through transistor 457 and diode 451 will flow through resistor 479. As discussed in detail above, current that flows through resistor 479 will result in the voltage drop across resistor 479, which results in a reduction in the maximum duty cycle of switching waveform 335. As the current that flows through resistor 479 increases, the maximum duty cycle of switching waveform 335 will be decreased.

Figure 5 is a diagram illustrating some of the currents, voltages and duty cycles associated with the power supply controller 139 in accordance with teachings of the present invention. In particular, diagram 501

illustrates when the power supply is enabled in relation to the input current of multi-function terminal 149. The x-axis represents the positive or negative current flowing into or out of multi-function terminal 149. As illustrated, as positive input current rises from zero and crosses over 50 microamps, power supply controller 139 in one embodiment is enabled. At this time, an under-voltage condition is removed. If the current is above 50 microamps but then falls below zero microamps, power supply controller 139 is disabled. At this time, an under-voltage condition is detected. The difference between 50 microamps and zero microamps provides hysteresis, which provides for more stable operation during noise or ripple conditions in the input current.

As the input current rises above 225 microamps, the power supply is disabled. At this time, an over-voltage condition is detected. When the input current falls back below 215 microamps, the power supply is re-enabled. At this time, the over-voltage condition is removed. The difference between 225 microamps and 215 microamps provides hysteresis, which provides for more stable operation during noise or ripple conditions in the input current.

Continuing with diagram 501, when the negative current that flows out from multi-function terminal 149 rises in magnitude to a level above 50 microamps, which is illustrated as -50 microamps in Figure 5, the power supply is enabled. At this time, the on/off feature of the present invention

turns on the power supply. When the negative current falls in magnitude to a level below 40 microamps, which is illustrated as -40 microamps in Figure 5, the power supply is disabled. At this time, the on/off feature of the present invention turns off the power supply. The difference between -50 microamps and -40 microamps provides hysteresis, which provides for more stable operation during noise or ripple conditions in the input current.

It is worthwhile to note that in one embodiment the positive input current is clamped at 300 microamps and that the negative input current is clamped at 200 microamps. The positive input current would be clamped at 300 microamps when, for example, the multi-function terminal 149 is short-circuited to a supply voltage. The negative input current would be clamped at 200 microamps when, for example, the multi-function terminal is short-circuited to ground.

In diagram 503, the current limit through power switch 147 as adjusted by the present invention is illustrated. Note that the hysteresis of the under-voltage and over-voltage conditions are illustrated from zero microamps to 50 microamps and from 215 microamps to 225 microamps, respectively. In one embodiment, when positive input current is provided into multi-function terminal 149 and there is neither an under-voltage condition nor an over-voltage condition, the current limit through power switch 147 is 3 amps. However, when negative current flows out from

multi-function terminal 149, and the magnitude of the negative current rises above 50 microamps, which is illustrated as -50 microamps in Figure 5, the current limit through power switch 149 is approximately 1 amp. As the magnitude of the negative current rises to 150 microamps, which is illustrated as -150 microamps in Figure 5, the current limit through power switch 149 rises proportionally with the negative current to 3 amps. After the magnitude of the negative current rises above 150 microamps, the current limit of the power switch 149 remains fixed at 3 amps. Note that there is also the on/off hysteresis between -50 microamps and -40 microamps in diagram 503.

Diagram 505 illustrates the maximum duty cycle setting of power supply controller 139 in relation to the input current. Note that the hysteresis from -50 microamps to -40 microamps, from zero microamps to 50 microamps and from to 215 microamps to 225 microamps as discussed above is included. In the embodiment illustrated in diagram 505, the maximum duty cycle is fixed at 75 percent until a positive input current of 60 microamps is reached. As the input current continues to increase, the maximum duty cycle continues to decrease until an input current of 225 microamps is reached, at which time the maximum duty cycle has been reduced to 33 percent. As illustrated, between 60 microamps and 225 microamps, the maximum duty cycle is inversely proportional to the positive input current. Note that when negative current

flows through multi-function terminal 149, and when the power supply is enabled, the maximum duty cycle in one embodiment is fixed at 75 percent.

Diagram 507 illustrates the voltage at multi-function terminal, which is labeled in diagram 507 as line sense voltage, in relation to the input current. When negative current is flowing from multi-function terminal 149, the voltage at multi-function terminal 149 is fixed at the band gap voltage V_{BG}, which in one embodiment is 1.25 volts. When positive current is flowing into multi-function terminal 149, the voltage at multi-function terminal is fixed at the band gap voltage V_{BG} plus a threshold voltage V_{TP}, which in one embodiment sum to 2.3 volts. In the event that a negative current having a magnitude of more than 200 microamps is attempted to be drawn out of the multi-function terminal 149, the voltage at multi-function terminal 149 drops to approximately zero volts. In the event that a positive current of more than 300 microamps flows into multi-function terminal 149, the voltage at multi-function terminal 149 rises. In this case, the voltage will be limited by either by a standard clamp used at the multi-function terminal for the purpose of protection or by the external circuitry driving the multi-function terminal, whichever is lower in voltage.

It is appreciated that the currents, voltages, duty cycle settings and hysteresis settings described in connection with the present invention are given for explanation purposes only and that other values may be

selected in accordance with teachings of the present invention. For example, in other embodiments, non hysteretic thresholds may be utilized. Thus the hysteresis values may be greater than or equal to zero.

Figure 6A is timing diagram illustrating one embodiment of some of the waveforms of a power supply controller in accordance with teachings of the present invention. Referring to both Figures 4 and 6A, oscillating waveform output 475 of oscillator 467 generates a sawtooth waveform, which is received by comparator 477. Oscillating waveform output 471 of oscillator 467 generates a maximum duty cycle signal, which is received by AND gate 493. Enable/disable signal 331, which is received at enable/disable input 469 of oscillator 467, is also illustrated. In Figure 6A, the enable/disable signal 331 is active. Therefore, the sawtooth waveform of oscillating waveform output 475 and the maximum duty cycle waveform of oscillating waveform output 471 are generated. Note that the sawtooth waveform and the maximum duty cycle waveform have the same frequency and period. One cycle of each of these waveform occurs between time 601 and time 605. The peak of the sawtooth waveform occurs at the same time as the rising edge of the maximum duty cycle waveform. This aspect is illustrated at time 601 and at time 605. The lowest point of the sawtooth waveform occurs at the same time as the falling edge of the maximum duty cycle waveform. This aspect is illustrated at time 603.

Referring now to Figure 6B, a timing diagram illustrating another embodiment of the waveforms of a power supply controller in accordance with teachings of the present invention is shown. From time 607 to time 609, the enable/disable signal 331 is low or inactive. In one embodiment, a low enable/disable signal 331 disables the power supply. A high or active enable/disable signal 331 enables the power supply. At time 609, the rising edge of enable/disable signal 331 occurs. At this time, oscillating waveform outputs 475 and 471 begin generating the sawtooth waveform and maximum duty cycle waveform, respectively. Note that a new complete cycle of each of these waveforms is generated in response to the rising edge of enable/disable signal 331 at time 609.

From time 609 to time 611, enable/disable signal 331 remains high or active. Thus, during this time, the sawtooth waveform and maximum duty cycle waveform are continuously generated.

At time 611, a falling edge of enable/disable signal 331 occurs. Before oscillator 467 discontinues generating the sawtooth waveform and the maximum duty cycle waveform, the existing cycles of each of these waveforms are allowed to complete. Stated differently, generation of the sawtooth waveform and the maximum duty cycle waveform is discontinued at a point just before the start of the on-time of the switching waveform 335 or the on- time of the power switch of the next cycle. This point in time is illustrated in Figure 6B at time 613. Note that after time

613, the sawtooth waveform remains inactive at a high value and the maximum duty cycle waveform remains inactive at a low value.

At time 615, another rising edge of enable/disable signal 331 occurs. Therefore, the sawtooth waveform and the maximum duty cycle waveform are generated beginning at a new complete cycle of each waveform. As illustrated in Figure 6B, a falling edge of enable/disable signal 331 occurs at time 617, which is immediately after the rising edge. However, the sawtooth waveform and maximum duty cycle waveforms are allowed to complete their then existing cycles. This occurs at time 619. After time 619, the waveforms remains inactive as shown during the time between time 619 and time 621, which is when another rising edge of enable/disable signal 331 occurs. At time 621, another new complete cycle of the sawtooth waveform and the maximum duty cycle waveform are generated. Since enable/disable signal 331 is deactivated at time 623, which occurs during a cycle of the sawtooth waveform and the maximum duty cycle waveform, these waveforms are deactivated after fully completing their respective cycles. Thus, by pulsing the on/off control signal at the multi-function terminal it is possible to synchronize the oscillator to the on/off pulse frequency.

Figure 7 is a schematic of another embodiment of a power supply controller 139 in accordance with the teachings of the present invention. The power supply controller schematic shown in Figure 7 is similar to the

power supply controller schematic discussed above in Figure 4. The primary difference between the power supply controller of Figures 4 and 7 is that oscillator 467 of Figure 7 does not have an enable/disable input 469 coupled to receive enable/disable signal 331. As shown in the embodiment depicted in Figure 7, the enable/disable signal 331 is used to directly gate the switching waveform at the input of AND gate 493. In this embodiment, the oscillator 467 is running all the time and switching waveform 335 will be gated on and off at any point in the cycle in response to the enable/disable signal 331.

To illustrate, Figure 8 shows one embodiment of timing diagrams of switching waveforms of the power supply controller illustrated in Figure 7. Referring to both Figures 7 and 8, oscillating waveform output 475 of oscillator 467 generates a sawtooth waveform, which is received by comparator 477. Oscillating waveform output 471 of oscillator 467 generates a maximum duty cycle signal, which is received by AND gate 493. Enable/disable signal 331, which is received by AND gate 493, and the output of AND gate 493, which is switching waveform 335, are also illustrated. In Figure 8, the enable/disable signal 331 is active only some of the time. Therefore, the switching waveform 335 is switching only during those portions of time that the enable/disable signal 331 is active. When the enable/disable signal 331 is not active, switching waveform 335 does not switch.

In the foregoing detailed description, the method and apparatus of the present invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.

CLAIMS

What is claimed is:

1. A power supply controller circuit, comprising a current input circuit coupled to receive a current representative of an input voltage, the current input circuit to generate an enable/disable signal when the current crosses a threshold having a hysteresis of greater than or equal to zero, the power supply controller to activate and deactivate the power supply in response to the enable/disable signal.

2. The power supply controller circuit of claim 1 further comprising an oscillator circuit coupled to the enable/disable signal, the oscillator circuit to start and stop generating a switching waveform in response to the enable/disable signal.

3. The power supply controller circuit of claim 2 wherein the oscillator circuit is to complete an existing cycle of the switching waveform before the oscillator is to stop generating the switching waveform in response to the enable/disable signal.

4. The power supply controller circuit of claim 2 wherein the oscillator circuit is to start a new complete cycle of the switching waveform if the oscillator circuit is to start generating the switching waveform in

response to the enable/disable signal.

5. The power supply controller circuit of claim 2 further comprising a power switch coupled to a primary winding of the power supply, the power switch coupled to receive and to switch in response to the switching waveform.

6. A power supply controller circuit, comprising a current input circuit coupled to receive a current representative of an input voltage, the current input circuit to generate an enable/disable signal to activate the power supply when the current is in between a first current threshold having a first hysteresis greater than or equal to zero and second current threshold having a second hysteresis greater than or equal to zero, the second current threshold higher than the first current threshold, the current input circuit to deactivate the power supply when the current is less than the first current threshold, the current input circuit to deactivate the power supply when the current is greater than the second current threshold.

7. The power supply controller circuit of claim 6 further comprising an oscillator circuit coupled to the enable/disable signal, the oscillator circuit to start and stop generating a switching waveform in response to the enable/disable signal.

8. The power supply controller circuit of claim 7 wherein the oscillator circuit is to complete an existing cycle of the switching waveform before the oscillator is to stop generating the switching waveform in response to the enable/disable signal.

9. The power supply controller circuit of claim 7 wherein the oscillator circuit is to start a new complete cycle of the switching waveform if the oscillator circuit is to start generating the switching waveform in response to the enable/disable signal.

10. The power supply controller circuit of claim 7 further comprising a power switch coupled to a primary winding of the power supply, the power switch coupled to receive and to switch in response to the switching waveform.

11. A power supply controller circuit, comprising a current input circuit coupled to receive a current representative of an on/off control signal applied to the power supply, the current input circuit to generate an enable/disable signal to activate the power supply when the current is in between a first current threshold having a first hysteresis greater than or equal to zero and second current threshold having a hysteresis greater than or equal to zero, the second current threshold higher than the first

current threshold, the current input circuit to deactivate the power supply when the current is less than the first current threshold, the current input circuit to deactivate the power supply when the current is greater than the second current threshold.

12. A power supply controller circuit, comprising:

a current input circuit coupled to receive a current representative of an input voltage applied to a power supply, the current input circuit to generate a maximum duty cycle adjustment signal in response thereto; and

a control circuit to generate a switching waveform, the control circuit coupled to receive the maximum duty cycle adjustment signal, the control circuit to limit the duty cycle of the switching waveform to a maximum value in response to the maximum duty cycle adjustment signal, the switching waveform to regulate the power supply output.

13. The power supply controller circuit of claim 12 further comprising a power switch coupled to a primary winding of the power supply, the power switch coupled to receive and to switch in response to the switching waveform.

14. The power supply controller circuit of claim 13 wherein the maximum duty cycle adjustment signal is inversely adjusted by the current

representative of the voltage input to the power supply when the current representative of the voltage input to the power supply is greater than a first value.

15. The power supply controller circuit of claim 14 wherein the maximum duty cycle adjustment signal is independent of the current representative of the voltage input to the power supply when the current representative of the voltage input to the power supply is less than the first value.

16. The power supply controller circuit of claim 12 wherein the maximum duty cycle adjustment signal is combined with a control signal received by the control circuit.

17. The power supply controller circuit of claim 16 wherein the control circuit is a pulse width modulation circuit that includes a comparator to compare an oscillating sawtooth waveform with the combined maximum duty cycle adjustment signal and the control signal received by the pulse width modulation circuit.

18. The power supply controller circuit of claim 17 wherein the duty cycle of the switching waveform is adjusted in response to an output of the comparator.

19. A power supply controller circuit, comprising a current input circuit coupled to receive a current representative of an on/off control signal applied to a power supply, the current input circuit to generate enable/disable signal when the current crosses an on/off threshold having a hysteresis greater than or equal to zero, the power supply controller to activate and deactivate a power supply in response to the on/off control signal.

20. The power supply controller circuit of claim 19 further comprising an oscillator circuit coupled to the enable/disable signal, the oscillator circuit to start and stop generating a switching waveform in response to the on/off control signal.

21. The power supply controller circuit of claim 20 wherein the oscillator circuit is to complete an existing cycle of the switching waveform before the oscillator is to stop generating the switching waveform in response to the on/off control signal.

22. The power supply controller circuit of claim 20 wherein the oscillator circuit is to start a new complete cycle of the switching waveform if the oscillator circuit is to start generating the switching waveform in response to the on/off control signal.

23. The power supply controller circuit of claim 20 further comprising a power switch coupled to a primary winding of the power supply, the power switch coupled to receive and to switch in response to the switching waveform.

24. The power supply controller circuit of claim 19 wherein the on/off threshold has a hysteresis greater than or equal to zero.

25. A power supply controller circuit, comprising:

a current input circuit coupled to receive a current, the current input circuit to generate an enable/disable signal to deactivate a power supply when the magnitude of current crosses below an on/off threshold having a hysteresis of greater than or equal to zero, the current input circuit to activate the power supply when the current crosses above the on/off threshold, the current input circuit to generate a current limit adjustment signal in response to the current; and

a control circuit coupled to receive the current limit adjustment signal, the control circuit coupled to adjust the current limit of a current through a power switch in response to the current limit adjustment signal.

26. The power supply controller circuit of claim 25 wherein the power switch is coupled to a primary winding of the power supply.

27. The power supply controller circuit of claim 26 wherein the control circuit is a pulse width modulation circuit that generates a switching waveform coupled to be received by the power switch to regulate the power supply output.

28. The power supply controller of claim 27 wherein the current is representative of a feedback signal from the power supply output, wherein the power supply voltage is regulated through current limit adjustment of the power switch in response to the feedback signal

29. A power supply controller circuit, comprising:

a current input circuit coupled to receive a current for adjusting a current limit of a power switch, the current input circuit to generate a current limit adjustment signal in response to the current; and

a control circuit coupled to receive the current limit adjustment signal, the control circuit coupled to adjust the current limit of a current through the power switch in response to the current limit adjustment signal.

30. The power supply controller circuit of claim 29 wherein the power switch is coupled to a primary winding of the power supply.

31. The power supply controller circuit of claim 29 wherein the control circuit is a pulse width modulation circuit that generates a switching waveform coupled to be received by the power switch to regulate the power supply output.

32. The power supply controller of claim 31 wherein the current is representative of a feedback signal from the power supply output, wherein the power supply voltage is regulated through current limit adjustment of the power switch in response to the feedback signal

33. The power supply controller of claim 31 wherein the control circuit includes a first comparator coupled to compare a voltage representative of the current through the power switch with the current limit adjustment signal such that the power switch is disabled in response to an output of the first comparator when the current limit set by the current limit adjustment signal is exceeded.

34. The power supply controller of claim 33 wherein the control circuit is to generate a switching waveform controlled in response to the output of the first comparator such that the switching waveform is coupled to limit the current through the power switch.

35. The power supply controller circuit of claim 29 wherein the

current limit of the current through the power switch is adjusted by the current when the current limit of the current through the power switch is below a predetermined maximum level.

36. The power supply controller circuit of claim 35 wherein the current limit of the current through the power switch is fixed at the predetermined maximum level for magnitudes of the currents that are higher than the current value corresponding to the predetermined maximum current limit level.

37. The power supply controller of claim 29, wherein the current circuit also generates an enable/disable signal that deactivates the power supply when the magnitude of the current is below an on/off threshold, the on/off threshold having a hysteresis of zero or greater.

38. The power supply controller circuit of claim 37 further comprising an oscillator circuit coupled to an enable/disable signal, the oscillator circuit to start and stop generating a switching waveform in response to the current crossing the on/off threshold.

39. The power supply controller circuit of claim 38 wherein the oscillator circuit is to complete an existing cycle of the switching waveform before the oscillator is to stop generating the switching waveform in

response to the enable/disable signal.

40. The power supply controller circuit of claim 38 wherein the oscillator circuit is to start a new complete cycle of the switching waveform if the oscillator circuit is to start generating the switching waveform in response to the enable/disable signal.

41. The power supply controller circuit of claim 29, wherein the current is received by the current input circuit on a low impedance terminal that has a reference voltage with respect to ground.

42. The power supply controller in claim 41, wherein the current limit of the power switch is set by the value of resistance connected between the reference voltage on the low impedance terminal and ground.

43. A method for controlling a power supply, comprising:

receiving a first current representative of an input voltage to the power supply through a first terminal of a power supply controller;

activating an under-voltage signal if the first current falls below a first under-voltage threshold value;

deactivating the under-voltage signal if the first current rises above a second under-voltage threshold value;

activating the power supply in response to a deactivated under-voltage signal; and

deactivating the power supply in response to an activated under-voltage signal.

44. The method of claim 43 wherein activating the switching waveform includes starting a new complete cycle of the switching waveform.

45. The method of claim 43 wherein deactivating the switching waveform includes allowing to complete an existing cycle of the switching waveform.

46. The method of claim 43 wherein the second under-voltage threshold value is greater than the first under-voltage threshold value.

47. The method of claim 43 further comprising generating a positive current sense signal in response to the first current.

48. The method of claim 43 wherein receiving the first current representative of the input voltage to the power supply comprises coupling a resistance between the first terminal and an input of the primary winding.

49. The method of claim 43 wherein activating the power supply in response to the deactivated under-voltage signal comprises enabling a switching waveform in response to the deactivated under-voltage signal, the switching waveform to control a power switch coupled to a primary winding of the power supply.

50. The method of claim 43 wherein deactivating the power supply in response to the activated under-voltage signal comprises disabling a switching waveform in response to the activated under-voltage signal, the switching waveform to control a power switch coupled to a primary winding of the power supply.

51. A method for controlling a power supply, comprising:

receiving a first current representative of an input voltage to the power supply through a first terminal of a power supply controller;

activating an over-voltage signal if the first current rises above a first over-voltage threshold value;

deactivating the over-voltage signal if the first current falls below a second over-voltage threshold value;

activating the power supply in response to a deactivated over-voltage signal; and

deactivating the power supply in response to an activated over-

voltage signal.

52. The method of claim 51 wherein activating the switching waveform includes starting a new complete cycle of the switching waveform.

53. The method of claim 51 wherein deactivating the switching waveform includes allowing to complete an existing cycle of the switching waveform.

54. The method of claim 51 wherein the first over-voltage threshold value is greater than the second over-voltage threshold value.

55. The method of claim 51 wherein receiving the first current representative of the input voltage to the power supply comprises coupling a resistance between the first terminal and an input of the primary winding.

56. The method of claim 51 further comprising switchably coupling the first terminal to a first potential to switchably generate an over-voltage condition.

57. The method of claim 51 wherein activating the power supply in

response to the deactivated over-voltage signal comprises enabling a switching waveform in response to the deactivated over-voltage signal, the switching waveform to control a power switch coupled to a primary winding of the power supply.

58. The method of claim 51 wherein deactivating the power supply in response to the activated over-voltage signal comprises disabling a switching waveform in response to the activated over-voltage signal, the switching waveform to control a power switch coupled to a primary winding of the power supply.

59. A method for controlling a power supply, comprising:

receiving a first current representative of an input voltage to the power supply through a first terminal of a power supply controller;

switching a second current flowing through the primary winding with a switching waveform having a duty cycle;

adjusting the duty cycle of the switching waveform in response to the first current.

60. The method of claim 59 wherein the limit to the duty cycle is reduced in response to an increase in the first current if the first current is greater than a first threshold value, the first threshold having a hysteresis of greater than or equal to zero.

61. The method of claim 60 further comprising leaving unchanged the duty cycle of the switching waveform if the first current is less than or equal to the first threshold value.

62. The method of claim 59 wherein adjusting the maximum duty cycle of the switching waveform comprises:

generating a positive current sense signal in response to the first current;

generating a first voltage in response to the positive current sense signal;

comparing the first voltage with a switching sawtooth waveform; and

resetting a latch to limit the maximum duty cycle of the switching waveform in response to comparing the first voltage with the switching sawtooth waveform.

63. The method of claim 59 wherein receiving the first current representative of the input voltage to the power supply comprises coupling a resistance between the first terminal and an input of the primary winding.

64. A method for controlling a power supply, comprising:

supplying a first current from a first terminal of a power supply controller;

deactivating the power supply if the first current supplied from the first terminal falls below a first threshold value; and

activating the power supply if the first current supplied from the first terminal rises above a second threshold value.

65. The method of claim 64 wherein deactivating the power supply comprises stopping a switching waveform to control a power switch coupled to a primary winding of the power supply.

66. The method of claim 64 wherein activating the power supply comprises starting a switching waveform to control a power switch coupled to a primary winding of the power supply

67. The method of claim 64 wherein the second threshold value is greater than the first threshold value.

68. The method of claim 64 further comprising limiting the first current supplied from the first terminal to a maximum value.

69. The method of claim 65 wherein stopping the switching waveform includes allowing to complete an existing cycle of the switching

waveform.

70. The method of claim 66 wherein starting the switching waveform includes starting a new complete cycle of the switching waveform.

71. The method of claim 64 further comprising coupling a switch between the first terminal and ground.

72. The method of claim 64 further comprising coupling a variable resistance between the first terminal and ground.

73. A method for controlling a power supply, comprising:

supplying a first current from a first terminal of a power supply controller;

controlling a second current flowing through a primary winding of the power supply with a power switch coupled to the primary winding; and

adjusting a current limit of the second current in response to the first current.

74. The method of claim 73 wherein adjusting the current limit of the second current comprises increasing the current limit of the second current in response to an increase in the first current.

75. The method of claim 73 wherein adjusting the current limit of the second current comprises decreasing the current limit of the second current in response to a decrease in the first current.

76. The method of claim 73 further comprising coupling a resistance between the first terminal and ground.

77. The method of claim 73 wherein controlling a second current flowing through the primary winding comprises:

switching the power switch in response to a switching waveform; and

adjusting the switching waveform in response to the first current.

78. The method of claim 77 wherein adjusting the switching waveform comprises:

generating a first voltage in response to the first current;

generating a second voltage in response to the second current; and

adjusting the switching waveform in response to a comparison of the first voltage and the second voltage.

79. A power supply controller, comprising:

a power switch having a drain terminal, a source terminal and a gate, the drain terminal coupled to a primary winding of a power supply and the source terminal coupled to ground;

a control circuit coupled to a control terminal, the drain terminal and the gate of the power switch, the control terminal coupled to an output of the power supply, the control circuit to generate a switching waveform to control the power switch;

multi-function circuitry coupled between a multi-function terminal and the control circuit, the switching waveform generated in response to the drain terminal, the control terminal and the multi-function terminal.

80. The power supply controller of claim 79 wherein the multi-function circuitry comprises:

a negative current sensor coupled to the multi-function terminal, the negative current sensor to generate a negative current sense signal in response to the multi-function terminal if a voltage at the multi-function terminal is less than a first voltage, the negative current sensor isolated from the multi-function terminal if the voltage at the multi-function terminal is greater than the first voltage;

a positive current sensor coupled to the multi-function terminal, the positive current sensor to generate a positive current sense signal in response to the multi-function terminal if the voltage at the multi-function terminal is greater than a second voltage, the positive current sensor

isolated from the multi-function terminal if the voltage at the multi-function terminal is less than the second voltage, wherein the second voltage is greater than the first voltage, the switching waveform generated in response to the negative current sense signal and the positive current sense signal.

81. The power supply controller of claim 80 wherein the multi-function circuitry further comprises on/off circuitry coupled to receive the negative current sense signal and coupled to the control circuit, the on/off circuitry to control the control circuit to start and to stop the switching waveform in response to the multi-function terminal.

82. The power supply controller of claim 80 wherein the multi-function circuitry further comprises external current limit adjuster circuitry coupled to receive the negative current sense signal and coupled to the control circuit, the external current limit adjuster circuitry control the control circuit to adjust a current limit of the power switch in response to a current received at the multi-function terminal.

83. The power supply controller of claim 80 wherein the multi-function circuitry further comprises under-voltage comparator circuitry coupled to receive the positive current sense signal and coupled to the control circuit, the under-voltage comparator circuitry to control the control

circuit to start and to stop the switching waveform in response to a current received at the multi-function terminal.

84. The power supply controller of claim 80 wherein the multi-function circuitry further comprises over-voltage comparator circuitry coupled to receive the positive current sense signal and coupled to the control circuit, the over-voltage comparator circuitry to control the control circuit to start and to stop the switching waveform in response to a current received at the multi-function terminal.

85. The power supply controller of claim 80 wherein the multi-function circuitry further comprises maximum duty cycle adjuster circuitry coupled to receive the positive current sense signal and coupled to the control circuit, the maximum duty cycle adjuster circuitry to adjust the maximum duty cycle of the switching waveform in response to a current received at the multi-function terminal.

86. The power supply controller of claim 79 wherein a voltage at the multi-function terminal is substantially equal to a first constant voltage if there is a negative current flowing through the multi-function terminal.

87. The power supply controller of claim 79 wherein a voltage at the multi-function terminal is substantially equal to a second constant

voltage if there is a positive current flowing through the multi-function terminal.

88. A method for controlling a power supply, comprising:

generating a switching waveform to control a power switch of a power supply controller coupled to a primary winding of the power supply;

adjusting the switching waveform in response to a drain terminal of the power supply controller coupled to the primary winding, a voltage at the drain terminal indicating a current flowing through the power switch;

adjusting the switching waveform in response to a control terminal of the power supply controller coupled to an output of the power supply; and

adjusting the switching waveform in response to a current flowing through a multi-function terminal of the power supply controller.

89. The method of claim 88 wherein adjusting the switching waveform in response to the current flowing through the multi-function terminal comprises generating a negative current sense signal if the current flowing through the multi-function terminal flows out of the power supply controller from the multi-function terminal.

90. The method of claim 88 wherein adjusting the switching waveform in response to the current flowing through the multi-function

terminal comprises generating a positive current sense signal if the current flowing through the multi-function terminal flows into the power supply controller through the multi-function terminal.

91. The method of claim 89 further comprising starting and stopping the switching waveform in response to the negative current sense signal.

92. The method of claim 89 further comprising controlling the switching waveform to limit the current flowing through the power switch in response to the negative current sense signal.

93. The method of claim 90 further comprising starting and stopping the switching waveform in response to the positive current sense signal.

94. The method of claim 90 further comprising reducing a maximum duty cycle of the switching waveform in response to the positive current sense signal.

95. The method of claim 89 further comprising coupling the multi-function terminal to ground through a resistance.

96. The method of claim 89 further comprising switchably coupling the multi-function terminal to ground.

97. The method of claim 90 further comprising coupling the multi-function terminal to an input voltage of the power supply through a resistance.

98. The method of claim 90 further comprising switchably coupling the multi-function terminal to a first potential.

99. The power supply controller, comprising:

a power switch coupled between a drain terminal and a source terminal, the drain terminal to be coupled to a primary winding of a power supply;

a control circuit coupled to the power switch, the drain terminal and a control terminal, the control terminal to be coupled to an output of the power supply;

a negative current sensor coupled to a multi-function terminal;

a positive current sensor coupled to the multi-function terminal;

a on/off circuit coupled between the negative current sensor and the control circuit;

an external current limit adjuster coupled between the negative current sensor and the control circuit;

an under-voltage comparator coupled between the positive current sensor and the control circuit;

an over-voltage comparator coupled between the positive current sensor and the control circuit; and

a maximum duty cycle adjuster coupled between the positive current sensor and the control circuit.

100. The power supply controller of claim 99 further comprising enable/disable logic coupled to an output of the under-voltage comparator, to an output of the over-voltage comparator, to an output of the on/off circuit and to an input of the control circuit.

101. The power supply controller of claim 99 wherein the power switch comprises a power transistor coupled between the drain terminal and the source terminal, the power transistor having a gate coupled to the control circuit.

102. The power supply controller of claim 99 wherein the negative current sensor comprises:

a first current source coupled to the control terminal;

a first transistor having a source coupled to the first current source and a gate coupled to a drain of the first transistor;

a second transistor having a source coupled to the source of the

first transistor and a gate coupled to the gate of the first transistor;

a third transistor having a drain coupled to the drain and the gate of the first transistor and to the gate of the second transistor, the third transistor having a source coupled to the multi-function terminal and a gate coupled to a first voltage; and

a fourth transistor having a drain and gate coupled to the drain of the second transistor.

103. The power supply controller of claim 102 wherein the on/off circuit comprises:

a second current source coupled to the control terminal; and

a fifth transistor having a gate coupled to the gate and drain of the fourth transistor and a drain coupled to the second current source.

104. The power supply controller of claim 102 wherein the external current limit adjuster comprises:

a third current source coupled to the control terminal;

a fourth current source coupled to the control terminal;

a sixth transistor having a gate coupled to the gate and drain of the fourth transistor and a drain coupled to the third current source;

a seventh transistor having a gate and drain coupled to the drain of the sixth transistor;

an eighth transistor having a gate coupled to the gate and drain of

the seventh transistor, the eighth transistor having a drain coupled to the fourth current source; and

a first resistor coupled to the fourth current source and the drain of the eighth transistor.

105. The power supply controller of claim 99 wherein the positive current sensor comprises:

a ninth transistor having a source coupled to the multi-function terminal and a gate coupled to a second voltage;

a tenth transistor having a gate and drain coupled to a drain of the ninth transistor;

an eleventh transistor having a gate coupled to the gate and drain of the tenth transistor;

a twelfth transistor having a source coupled to the control terminal and a gate and drain coupled to a drain of the eleventh transistor; and

a fifth current source coupled to a source of the tenth transistor and coupled to a source of the eleventh transistor.

106. The power supply controller of claim 105 wherein the under-voltage comparator comprises:

a thirteenth transistor having a source coupled to the control terminal and having a gate coupled to the gate and drain of the twelfth transistor; and

a sixth current source coupled to a drain of the thirteenth transistor.

107. The power supply controller of claim 105 wherein the over-voltage comparator comprises:

the fourteenth transistor having a source coupled to the control terminal and having a gate coupled to the gate and drain of the twelfth transistor; and

a seventh current source coupled to a drain of the fourteenth transistor.

108. The power supply controller of claim 100 wherein the enable/disable logic comprises:

a first NOR gate having a first input coupled to the under-voltage comparator and having an inverted second input coupled to the on/off circuit; and

a second NOR gate having a first input coupled to the over-voltage comparator and having a second input coupled to an output of the first NOR gate.

109. The power supply controller of claim 105 wherein the maximum duty cycle adjuster comprises:

a fifteenth transistor having a source coupled to the control terminal and having a gate coupled to the gate and drain of the twelfth transistor;

a first diode coupled to a drain of the fifteenth transistor; and

an eighth current source coupled to the drain of the fifteenth transistor.

110. The power supply controller of claim 100 wherein the control circuit comprises:

a second resistor coupled to the control terminal;

a sixteenth transistor having a source coupled to the second resistor and a drain coupled to the maximum duty cycle adjuster;

a first comparator having a first input coupled to the source of the sixteenth transistor and the second resistor, the first comparator having a second input coupled to a third voltage;

a third resistor coupled to the drain of the sixteenth transistor;

a fourth resistor coupled to the drain of the sixteenth transistor and the third resistor;

a first capacitor coupled to the fourth resistor;

an oscillator having an enable/disable input and first, second and third switching waveform outputs, the enable/disable input of the oscillator coupled to the enable/disable logic;

a fifth resistor coupled to the drain terminal;

a sixth resistor coupled to the fifth resistor;

a second comparator having a first input coupled to the fifth and sixth resistors and a second input coupled to the external current limit

adjuster;

a third comparator having a first input coupled to the third switching waveform output and having a second input coupled to the first capacitor and the fourth resistor;

a leading edge blanking delay circuit coupled to the power switch;

a first AND gate having a first input coupled to the leading edge blanking delay circuit and having a second input coupled to an output of the second comparator;

a first OR gate having a first input coupled to an output of the first AND gate and having a second input coupled to an output of the third comparator;

a first latch having a set input coupled to the second switching waveform output and having a reset input coupled to an output of the first OR gate; and

a second AND gate having a first input coupled to the first switching waveform output and having a second input coupled to an output of the first latch, the second AND gate having an output coupled to the power switch.

111. The power supply controller of claim 110 wherein the oscillator begins generating new complete cycles of first, second and third switching waveforms at the first, second and third switching waveform outputs, respectively, in response to an enable/disable signal received at

the enable/disable input.

112. The power supply controller of claim 110 wherein the oscillator allows to complete existing cycles of first, second and third switching waveforms at the first, second and third switching waveform outputs, respectively, before stopping the first, second and third switching waveforms in response to an enable/disable signal received at the enable/disable input.

ABSTRACT OF THE DISCLOSURE

A power supply controller having a multi-function terminal. In one embodiment, a power supply controller for switched mode power supply includes a drain terminal, a source terminal, a control terminal and a multi-function terminal. The multi-function terminal may be configured in a plurality of ways providing any one or some of a plurality of functions including on/off control, external current limit adjustments, under-voltage detection, over-voltage detection and maximum duty cycle adjustment. The operation of the multi-function terminal varies depending on whether a positive or negative current flows through the multi-function terminal. A short-circuit to ground from the multi-function terminal enables the power supply controller. A short-circuit to a supply voltage from the multi-function terminal disables the power supply controller. The current limit of an internal power switch of the power supply controller may be adjusted by externally setting a negative current from the multi-function terminal. The multi-function terminal may also be coupled to the input DC line voltage of the power supply through a resistance to detect an under-voltage condition, an over-voltage condition and/or adjust the maximum duty cycle of power supply controller. Synchronization of the oscillator of the power supply controller may also be realized by switching the multi-function terminal to power or ground at the desired times.

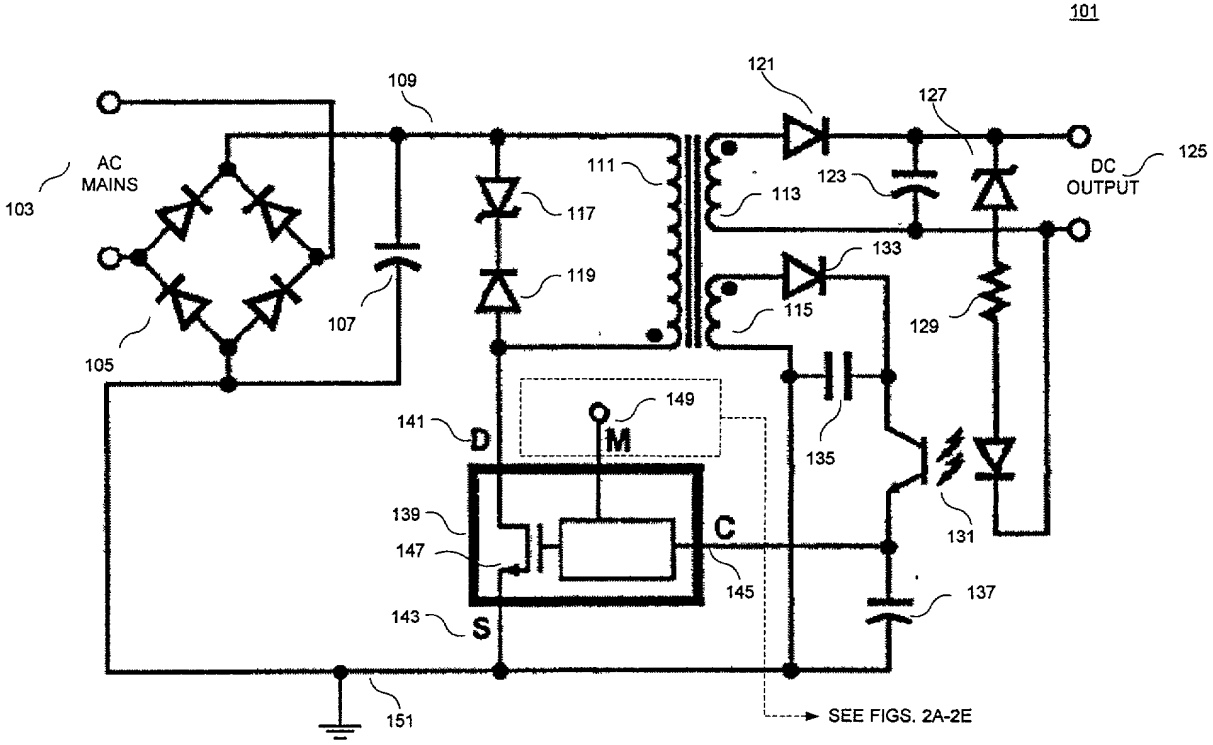

101
AC MAINS
103
105
107
109
111
113
115
117
119
121
123
125
DC OUTPUT
127
129
131
133
135
137
139
141
143
145
147
149
151
D
M
C
S
SEE FIGS. 2A-2E

FIG. 1

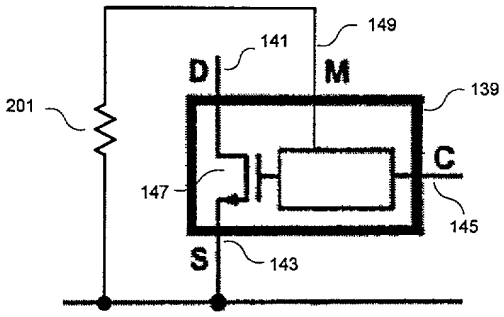


FIG. 2A

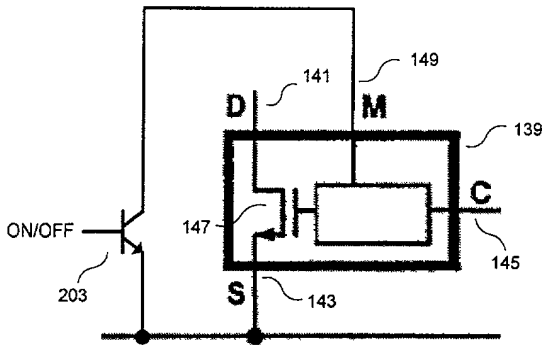


FIG. 2B

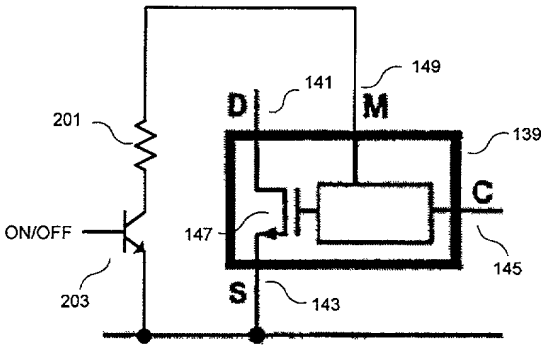


FIG. 2C

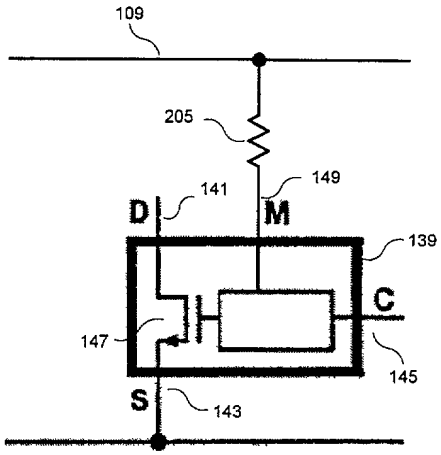


FIG. 2D

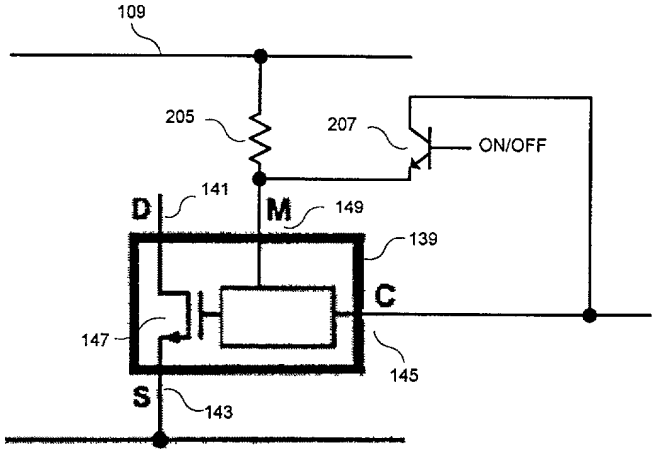


FIG. 2E

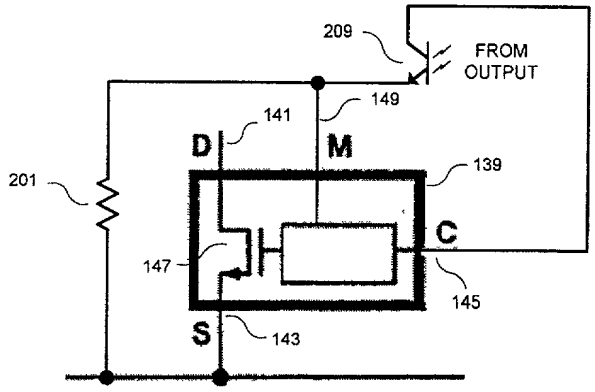


FIG. 2F

139

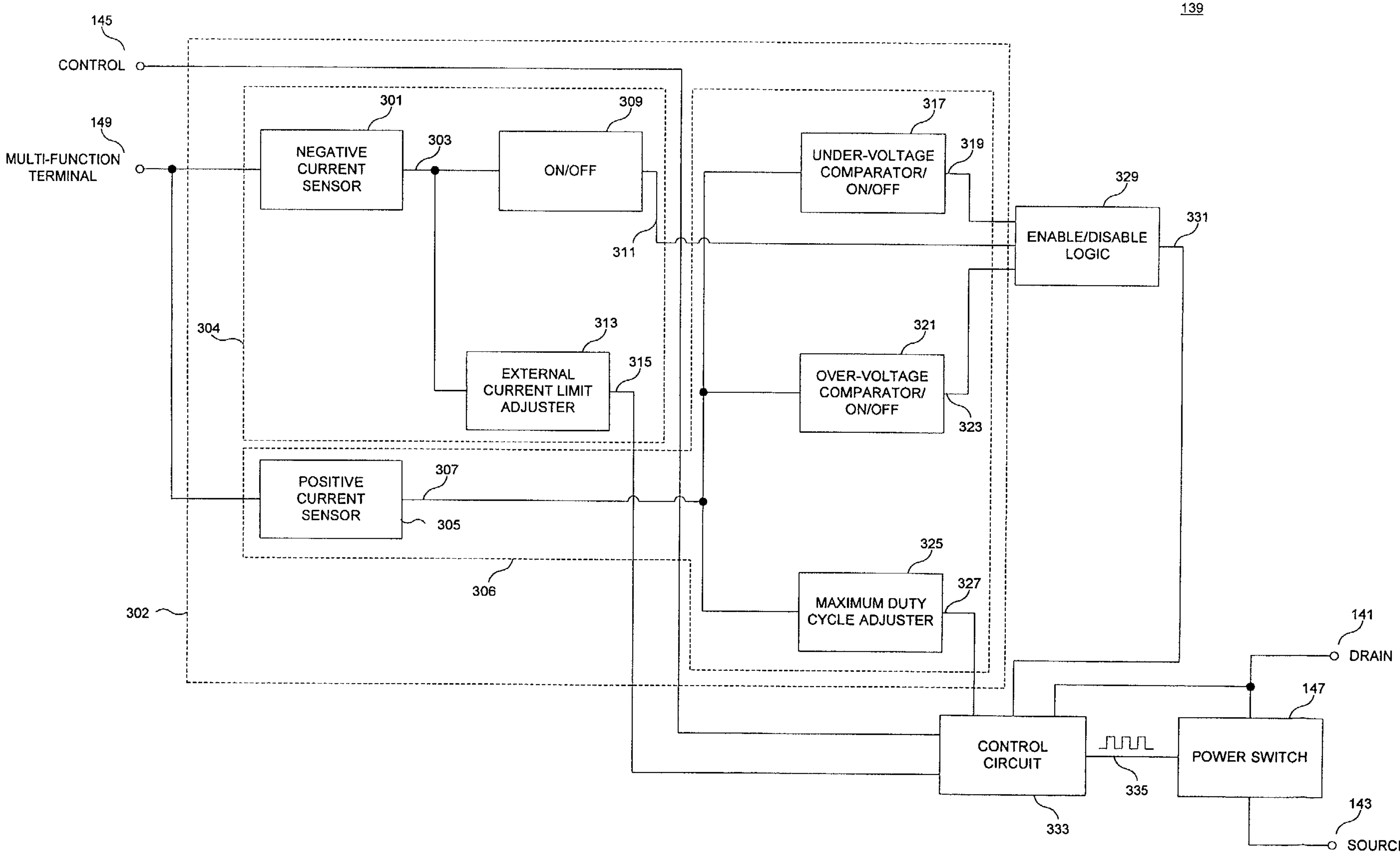

145
CONTROL
149
MULTI-FUNCTION TERMINAL
301
NEGATIVE CURRENT SENSOR
303
309
ON/OFF
311
304
313
EXTERNAL CURRENT LIMIT ADJUSTER
315
307
POSITIVE CURRENT SENSOR
305
306
302
317
UNDER-VOLTAGE COMPARATOR/ ON/OFF
319
321
OVER-VOLTAGE COMPARATOR/ ON/OFF
323
325
MAXIMUM DUTY CYCLE ADJUSTER
327
329
ENABLE/DISABLE LOGIC
331
CONTROL CIRCUIT
333
335
147
POWER SWITCH
141
DRAIN
143
SOURCE

FIG. 3

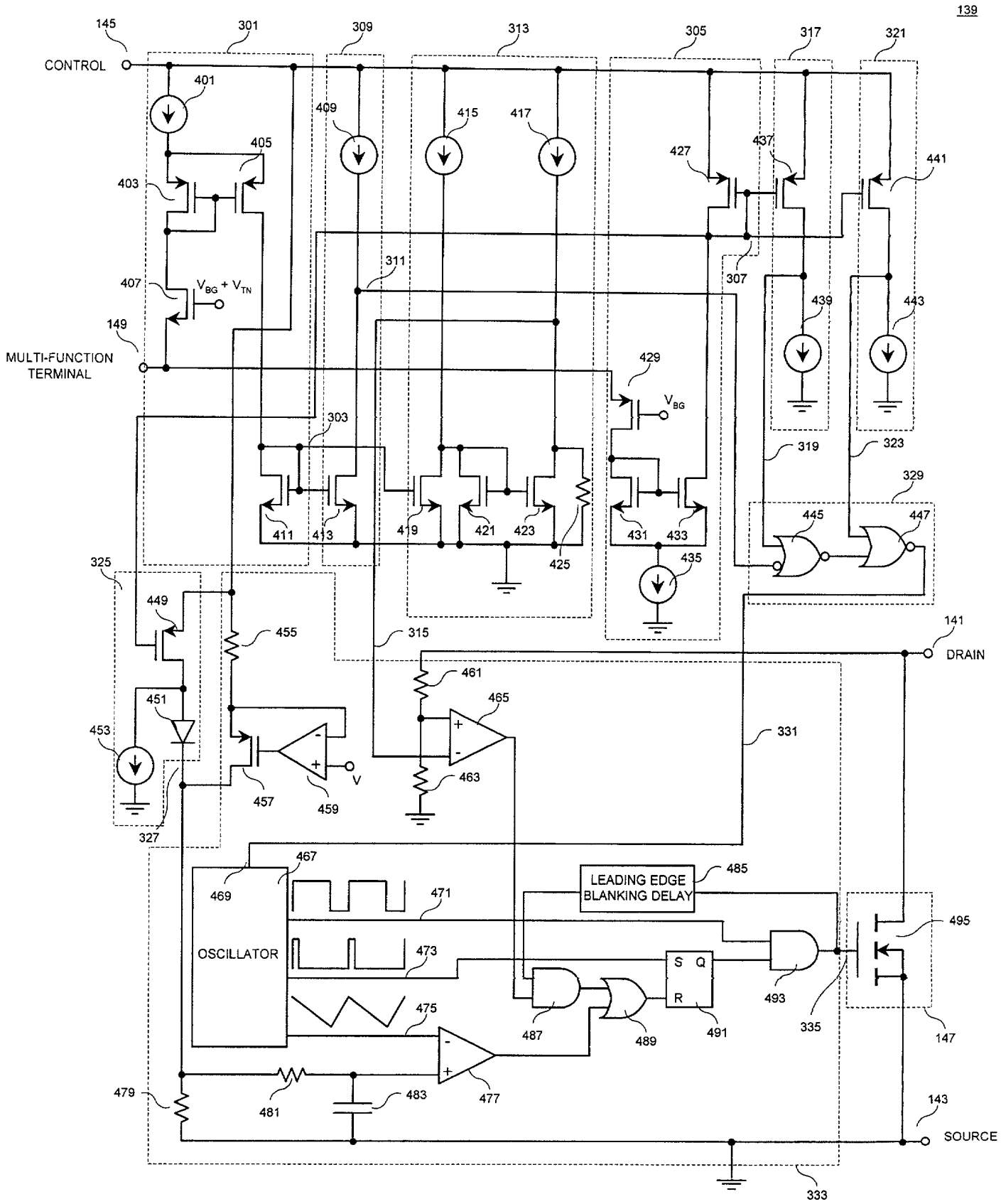

139
145
CONTROL
301
309
313
305
317
321
401
409
415
417
405
403
427
437
441
311
307
407
$V_{BG} + V_{TN}$
439
443
149
MULTI-FUNCTION TERMINAL
429
V_{BG}
303
319
323
329
411
413
419
421
423
425
431
433
435
445
447
325
449
455
315
141
DRAIN
461
451
465
453
331
457
459
V
463
327
467
469
471
LEADING EDGE BLANKING DELAY
485
OSCILLATOR
473
S Q
R
493
495
475
487
489
491
335
147
477
479
481
483
143
SOURCE
333

FIG. 4

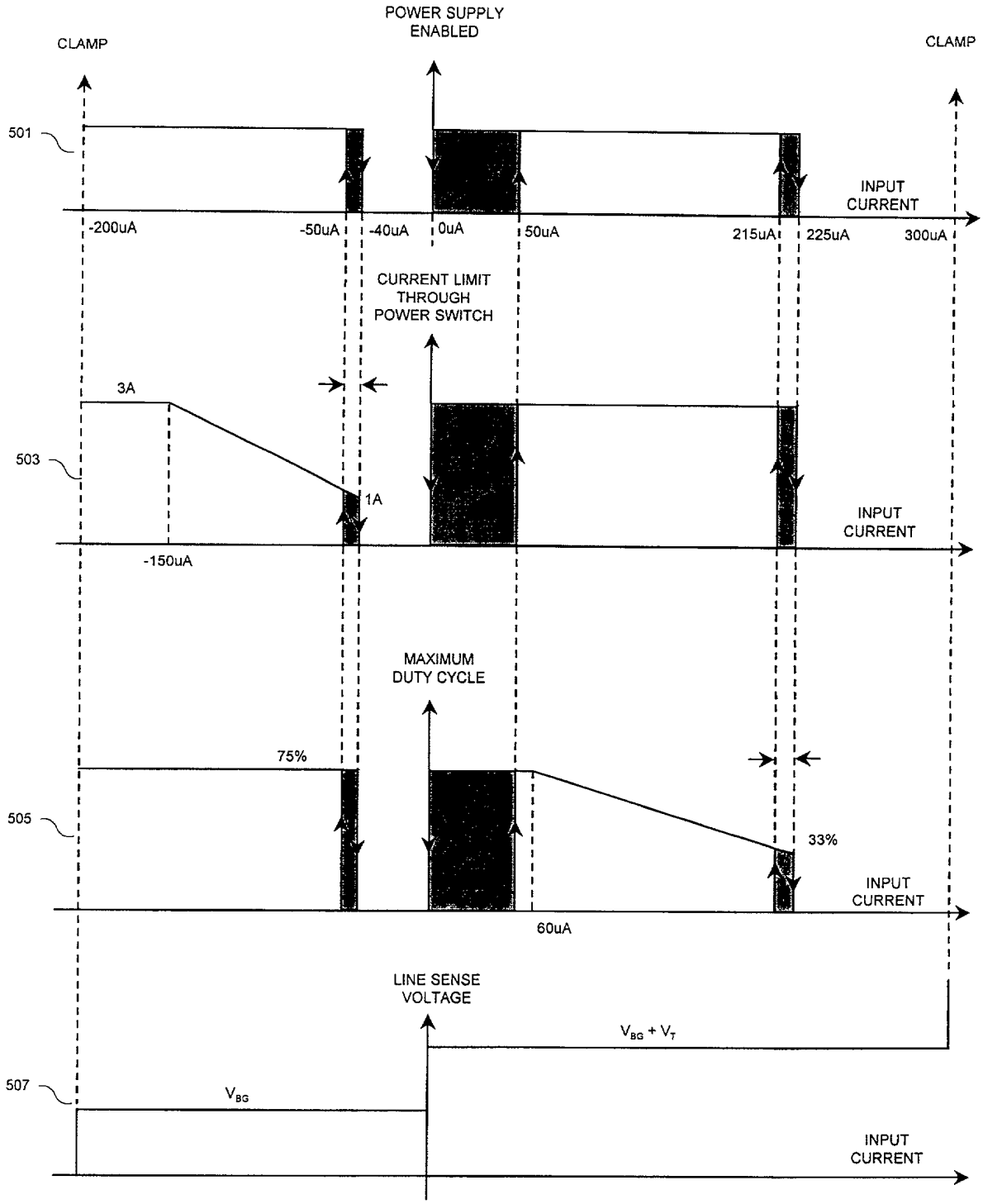

POWER SUPPLY ENABLED
CLAMP
CLAMP
501
INPUT CURRENT
-200uA
-50uA
-40uA
0uA
50uA
215uA
225uA
300uA
CURRENT LIMIT THROUGH POWER SWITCH
3A
503
1A
INPUT CURRENT
-150uA
MAXIMUM DUTY CYCLE
75%
505
33%
INPUT CURRENT
60uA
LINE SENSE VOLTAGE
$V_{BG} + V_T$
507
V_{BG}
INPUT CURRENT

FIG. 5

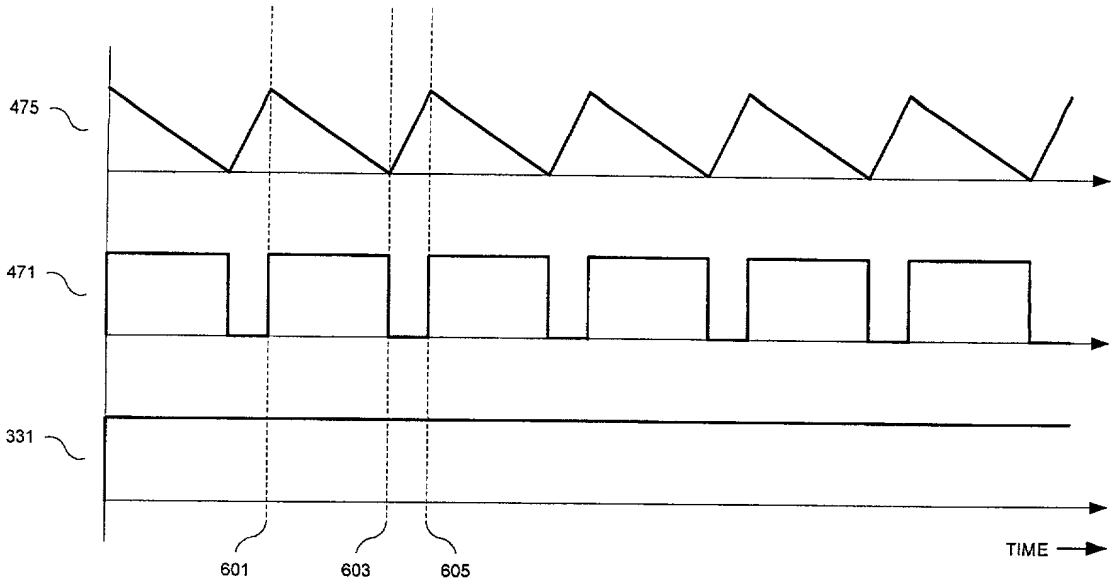

475
471
331
601
603
605
TIME

FIG. 6A

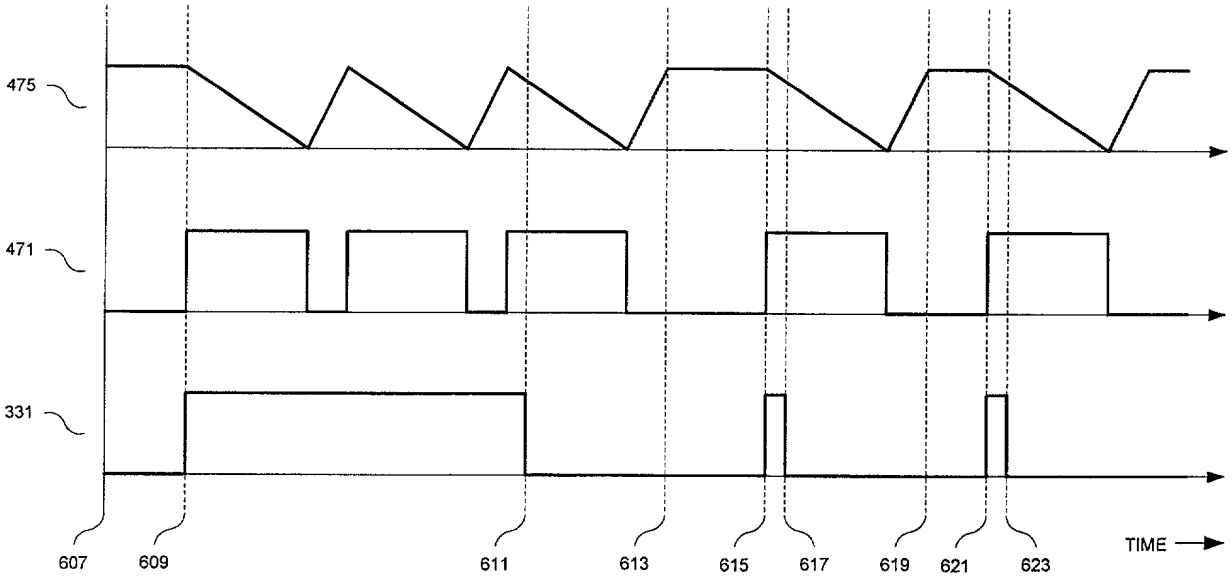
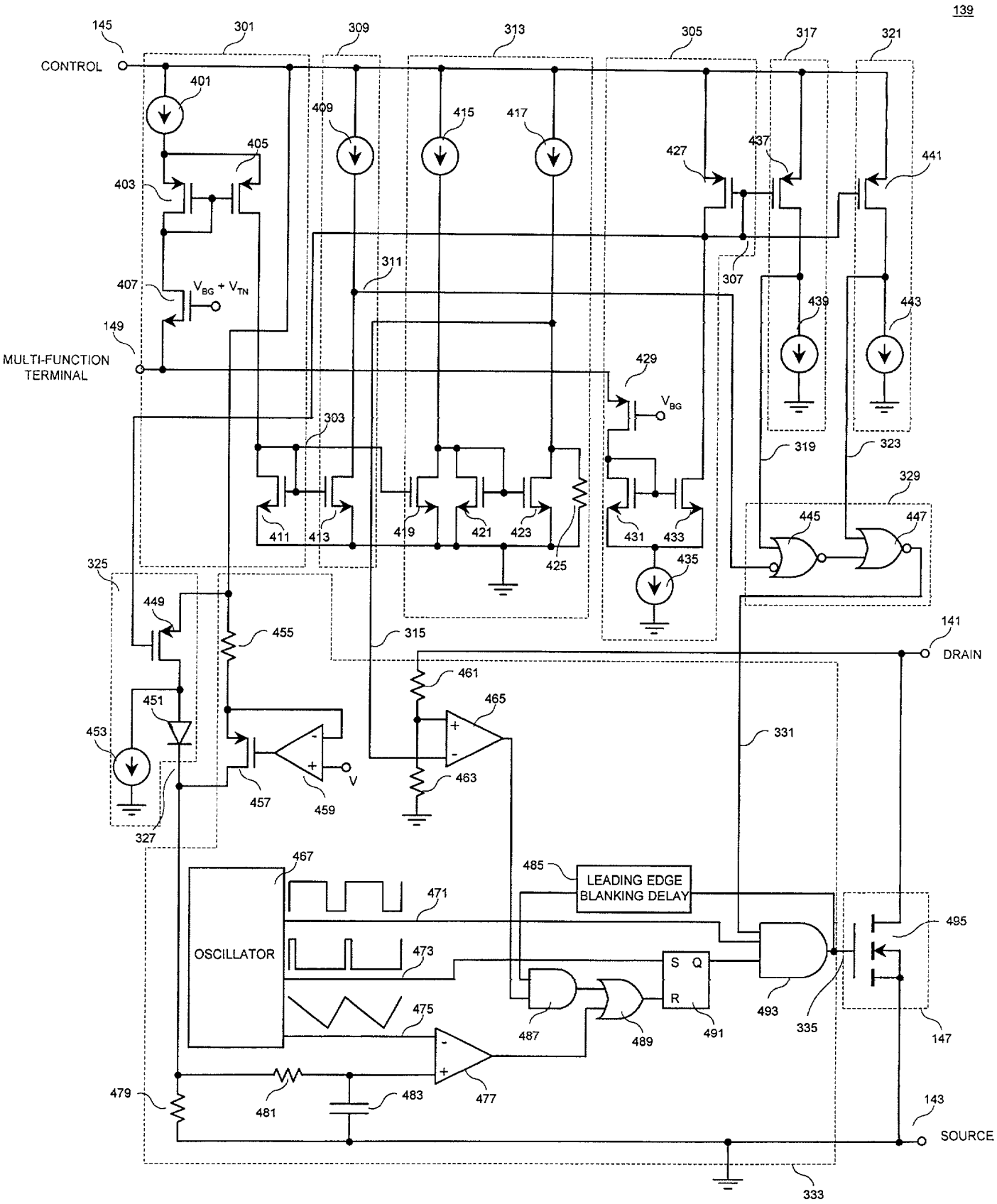

475
471
331
607
609
611
613
615
617
619
621
623
TIME

FIG. 6B


139
145
301
309
313
305
317
321
CONTROL
401
405
403
409
415
417
427
437
441
311
307
407
$V_{BG} + V_{TN}$
149
MULTI-FUNCTION TERMINAL
439
443
429
V_{BG}
303
319
323
329
411
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DRAIN
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327
467
485
LEADING EDGE BLANKING DELAY
471
OSCILLATOR
473
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143
SOURCE
333

FIG. 7

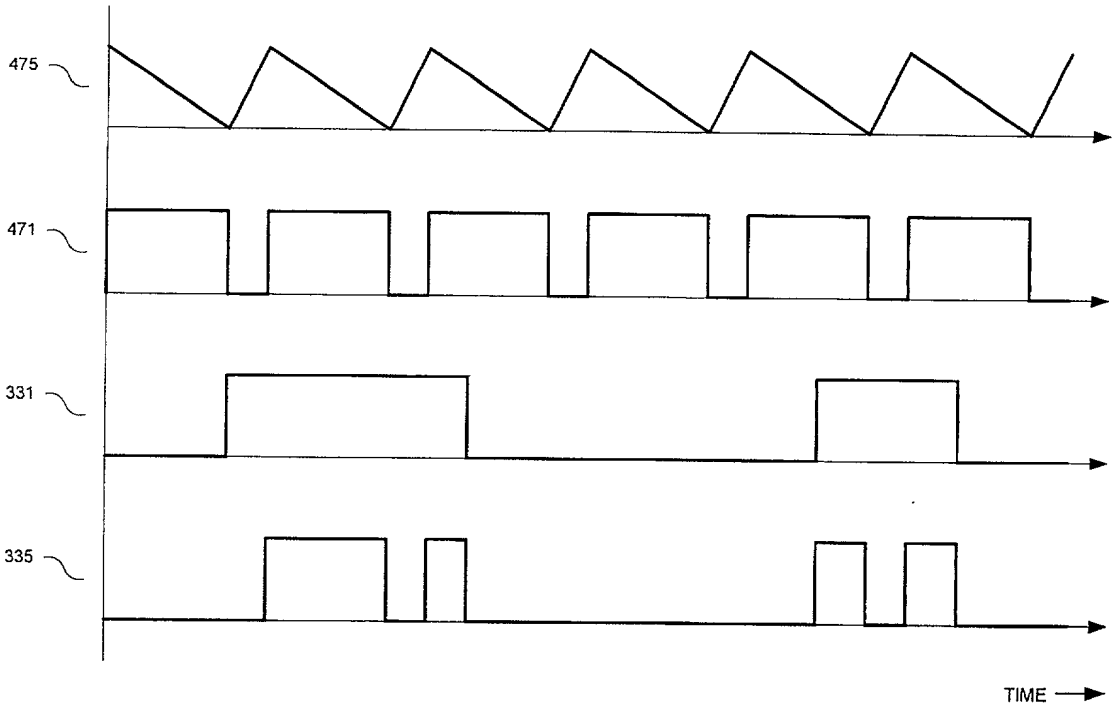

FIG. 8

Attorney's Docket No.: 003692.P040 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTOLLER

the specification of which

_X_ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
Number	Country	Day/Month/Year Filed	Yes	No
Number	Country	Day/Month/Year Filed	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to James Y. Go (Name of Attorney or Agent), **BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** James Y. Go (Name of Attorney or Agent), **(408) 720-8598.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature Leif O. Lund Date 9-23-1999.

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Full Name of Fourth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Fifth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Sixth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Seventh/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.